

SHEET

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SHEET

TITLE

30	FP,F_USB,BZ
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33	DVI
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45	TABLE LIST

PH7 PH8 PH1 PH2 PH9 PH10 PH3

PH4

PH11

PH12

PH5

PH6

CPU SOCKET

2 oz PCB

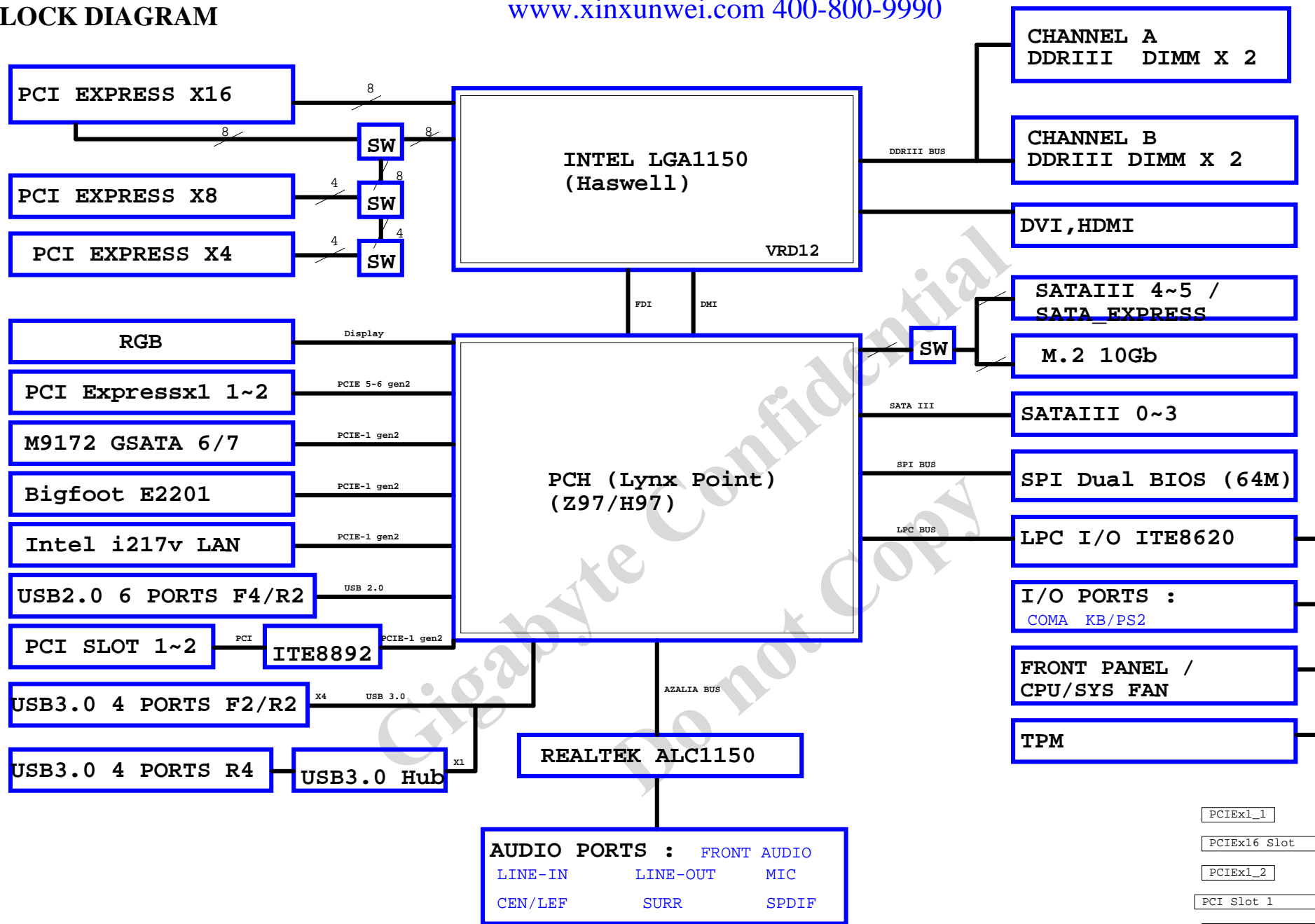
Gigabyte Technology

Title			
Cover Sheet			
Size	Document Number	GA-Z97X-UD5H	Rev 1.11
Custom			
Date:	Wednesday, July 16, 2014	Sheet 1	of 45



# BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990



PCIEx1\_1

PCIEx16 Slot

PCIEx1\_2

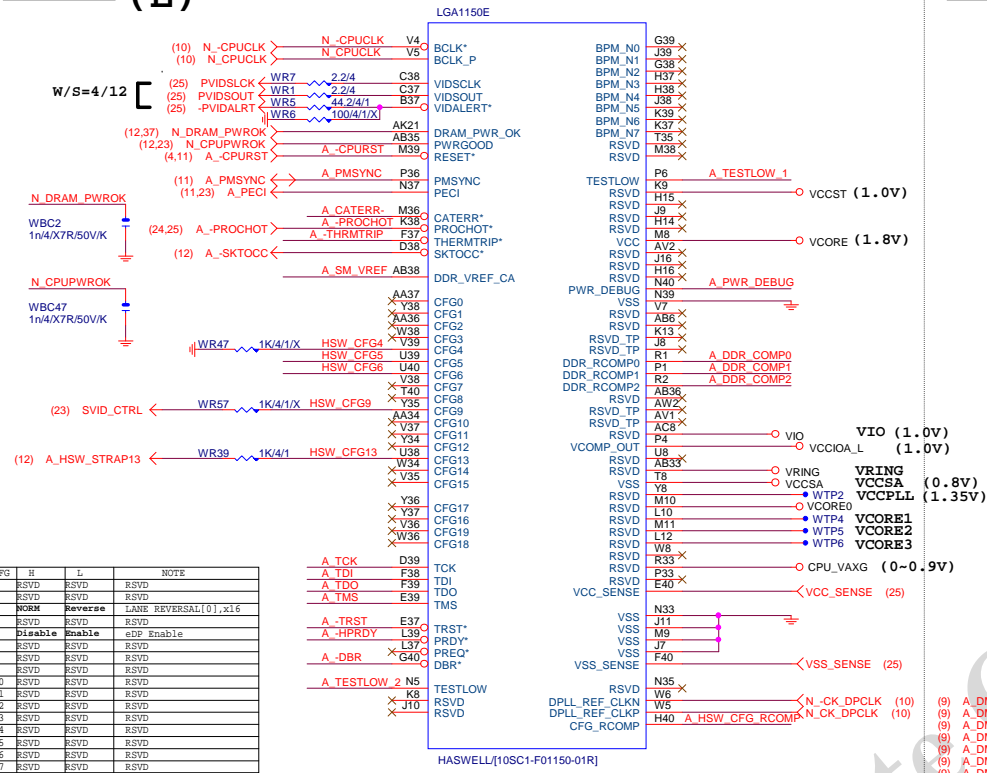
PCI Slot 1

PCIEx8

PCI Slot 2

PCIEx4

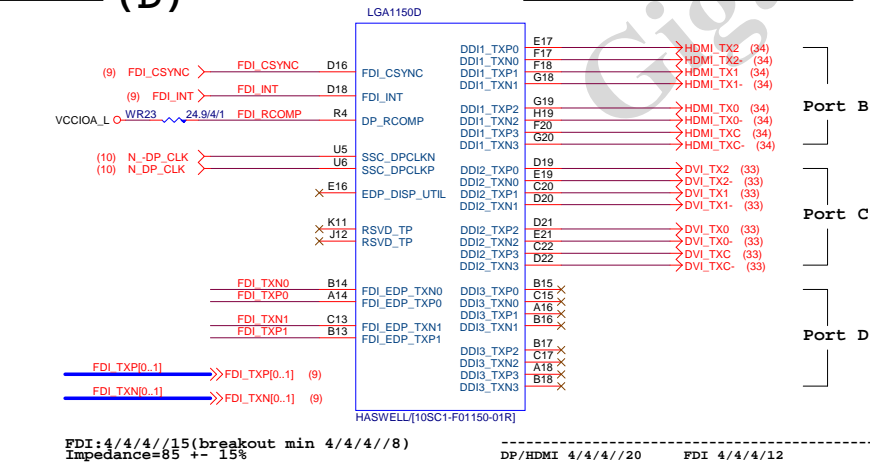
## LGA1150 (E)



CFG	H	L	NOTE
0	RSVD	RSVD	
1	RSVD	RSVD	
2	NORM	Reverse	LANE REVERSAL[0].x16
3	RSVD	RSVD	
4	Variable	Enable	eDP Enable
7	RSVD	RSVD	
8	RSVD	RSVD	
9	RSVD	RSVD	
10	RSVD	RSVD	
11	RSVD	RSVD	
12	RSVD	RSVD	
13	RSVD	RSVD	
14	RSVD	RSVD	
15	RSVD	RSVD	
16	RSVD	RSVD	
17	RSVD	RSVD	

CFG 0-17 all internal PULL-UP

## LGA1150 (D)

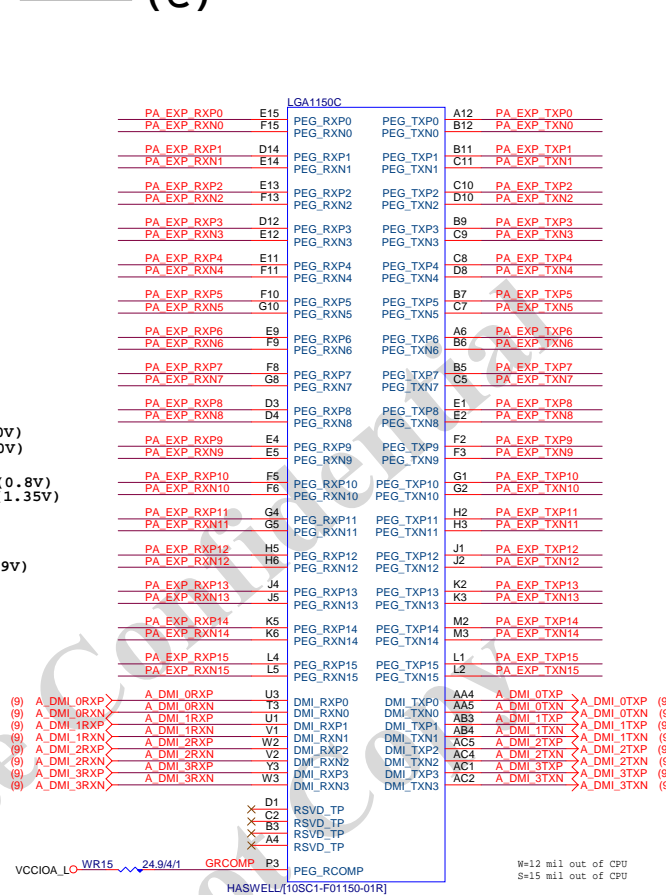


## HDMI 需接 Port B for WHQL

DP/HDMI 4/4/4/20 FDI 4/4/4/12

Impedance=85 +- 15%

## LGA1155 (C)



CPU PEG 5/5/5/20 Impedance=80 +- 15%

DMI 4/4/4/15 Impedance=85 +- 15%

## -CPURST

1.1V分壓

Remove分壓電阻

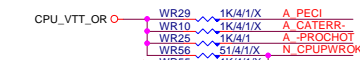
A-CPURST (4,11)

WBC3 1n4/7R/50V/K

## CPU SVID



## CPU PU/PD



A-THRMTRIP WR70 1K4/1 VCC1\_05\_PCH

WR34 150/4/1 VCC1\_05\_PCH

A-PWR\_DEBUG WR33 8.2K/4/X

A-DBR WR20 0/4/X N-SYS\_RST (12,30)

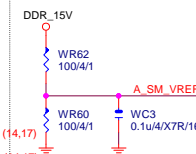
A-DDR\_COMP0 WR28 100/4/1

A-DDR\_COMP2 WR22 100/4/1

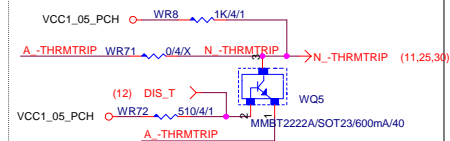
A-TESTLOW\_1 WR18 49.9/4/1

A-TESTLOW\_2 WR12 49.9/4/1

A-HSW\_CFG\_RCOMP WR24 49.9/4/1



## THRMTRIP DISABLE FOR Z87 OVERCLOCK



## Gigabyte Technology

Title			
CPU LGA1150-A			
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.11	
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LGA1150

(A)

LGA1150A			
MAAA0	AU13	DDR0_MA0	DDR0_DQ0
MAAA1	AV16	DDR0_MA1	DDR0_DQ1
MAAA2	AU16	DDR0_MA2	DDR0_DQ2
MAAA3	AW17	DDR0_MA3	DDR0_DQ3
MAAA4	AU17	DDR0_MA4	DDR0_DQ4
MAAA5	AW18	DDR0_MA5	DDR0_DQ5
MAAA6	AV17	DDR0_MA6	DDR0_DQ6
MAAA7	AT18	DDR0_MA7	DDR0_DQ7
MAAA8	AU18	DDR0_MA8	DDR0_DQ8
MAAA9	AT19	DDR0_MA9	DDR0_DQ9
MAAA10	AW11	DDR0_MA10	DDR0_DQ10
MAAA11	AV19	DDR0_MA11	DDR0_DQ11
MAAA12	AU19	DDR0_MA12	DDR0_DQ12
MAAA13	AY10	DDR0_MA13	DDR0_DQ13
MAAA14	AT20	DDR0_MA14	DDR0_DQ14
MAAA15	AU21	DDR0_MA15	DDR0_DQ15
MODT_A0	AW10	DDR0_ODT0	DDR0_ODT0
MODT_A1	AY8	DDR0_ODT1	DDR0_ODT1
MODT_A2	AW9	DDR0_ODT2	DDR0_ODT2
MODT_A3	AU8	DDR0_ODT3	DDR0_ODT3
AW33		DDR0_ECC0	DDR0_ECC0
AV33		DDR0_ECC1	DDR0_ECC1
AU31		DDR0_ECC2	DDR0_ECC2
AV31		DDR0_ECC3	DDR0_ECC3
AT33		DDR0_ECC4	DDR0_ECC4
AU33		DDR0_ECC5	DDR0_ECC5
AT31		DDR0_ECC6	DDR0_ECC6
AW31		DDR0_ECC7	DDR0_ECC7
SBA0	AV12	DDR0_BA0	DDR0_BA0
SBA1	AY11	DDR0_BA1	DDR0_BA1
SBA2	AT21	DDR0_BA2	DDR0_BA2
CKEA0	AV22	DDR0_CKE0	DDR0_CKE0
CKEA1	AT23	DDR0_CKE1	DDR0_CKE1
CKEA2	AU22	DDR0_CKE2	DDR0_CKE2
CKEA3	AU23	DDR0_CKE3	DDR0_CKE3
CSA0	AU14	DDR0_CS_N0	DDR0_CS_N0
CSA1	AV9	DDR0_CS_N1	DDR0_CS_N1
CSA2	AU10	DDR0_CS_N2	DDR0_CS_N2
CSA3	AW8	DDR0_CS_N3	DDR0_CS_N3
DCLKA0	AY15	DDR0_CLK_P0	DDR0_CLK_P0
DCLKA0	AY16	DDR0_CLK_N0	DDR0_CLK_N0
DCLKA1	AW15	DDR0_CLK_P1	DDR0_CLK_P1
DCLKA1	AV15	DDR0_CLK_N1	DDR0_CLK_N1
DCLKA2	AW14	DDR0_CLK_P2	DDR0_CLK_P2
DCLKA2	AW14	DDR0_CLK_N2	DDR0_CLK_N2
DCLKA3	AW13	DDR0_CLK_P3	DDR0_CLK_P3
DCLKA3	AY13	DDR0_CLK_N3	DDR0_CLK_N3
AW12		RSVD	
RSVD		DDR0_RAS*	DDR0_RAS*
RSVD		DDR0_WE*	DDR0_WE*
RSVD		DDR0_DQS_P0	DDR0_DQS_P0
RSVD		DDR0_DQS_P1	DDR0_DQS_P1
RSVD		DDR0_DQS_P2	DDR0_DQS_P2
RSVD		DDR0_DQS_P3	DDR0_DQS_P3
RSVD		DDR0_DQS_P4	DDR0_DQS_P4
RSVD		DDR0_DQS_P5	DDR0_DQS_P5
RSVD		DDR0_DQS_P6	DDR0_DQS_P6
RSVD		DDR0_DQS_P7	DDR0_DQS_P7
RSVD		DDR0_DQS_P8	DDR0_DQS_P8
RSVD		DDR0_DQS_N0	DDR0_DQS_N0
RSVD		DDR0_DQS_N1	DDR0_DQS_N1
RSVD		DDR0_DQS_N2	DDR0_DQS_N2
RSVD		DDR0_DQS_N3	DDR0_DQS_N3
RSVD		DDR0_DQS_N4	DDR0_DQS_N4
RSVD		DDR0_DQS_N5	DDR0_DQS_N5
RSVD		DDR0_DQS_N6	DDR0_DQS_N6
RSVD		DDR0_DQS_N7	DDR0_DQS_N7
RSVD		DDR0_DQS_N8	DDR0_DQS_N8

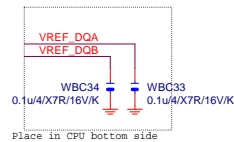
HASWELL[10SC1-F01150-01R]

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LGA1150

(B)

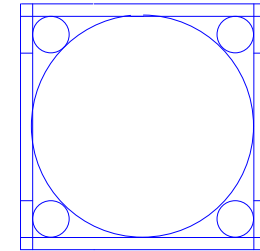
LGA1150B			
MAAB0	AL19	DDR1_MA0	DDR1_DQ0
MAAB1	AK23	DDR1_MA1	DDR1_DQ1
MAAB2	AM22	DDR1_MA2	DDR1_DQ2
MAAB3	AM23	DDR1_MA3	DDR1_DQ3
MAAB4	AP23	DDR1_MA4	DDR1_DQ4
MAAB5	AL23	DDR1_MA5	DDR1_DQ5
MAAB6	AY24	DDR1_MA6	DDR1_DQ6
MAAB7	AV25	DDR1_MA7	DDR1_DQ7
MAAB8	AU26	DDR1_MA8	DDR1_DQ8
MAAB9	AW25	DDR1_MA9	DDR1_DQ9
MAAB10	AP18	DDR1_MA10	DDR1_DQ10
MAAB11	AY25	DDR1_MA11	DDR1_DQ11
MAAB12	AV26	DDR1_MA12	DDR1_DQ12
MAAB13	AR15	DDR1_MA13	DDR1_DQ13
MAAB14	AY27	DDR1_MA14	DDR1_DQ14
MAAB15	AY28	DDR1_MA15	DDR1_DQ15
MODT_B0	AM17	DDR1_ODT0	DDR1_ODT0
MODT_B1	AL18	DDR1_ODT1	DDR1_ODT1
MODT_B2	AM16	DDR1_ODT2	DDR1_ODT2
MODT_B3	AK15	DDR1_ODT3	DDR1_ODT3
AM26		DDR1_ECC0	DDR1_ECC0
AM25		DDR1_ECC1	DDR1_ECC1
AP25		DDR1_ECC2	DDR1_ECC2
AP26		DDR1_ECC3	DDR1_ECC3
AL26		DDR1_ECC4	DDR1_ECC4
AL25		DDR1_ECC5	DDR1_ECC5
AR26		DDR1_ECC6	DDR1_ECC6
AR25		DDR1_ECC7	DDR1_ECC7
SBA0	AK17	DDR1_BA0	DDR1_BA0
SBA1	AL18	DDR1_BA1	DDR1_BA1
SBA2	AW28	DDR1_BA2	DDR1_BA2
CKEB0	AW29	DDR1_CKE0	DDR1_CKE0
CKEB1	AU29	DDR1_CKE1	DDR1_CKE1
CKEB2	AU28	DDR1_CKE2	DDR1_CKE2
CKEB3	AU29	DDR1_CKE3	DDR1_CKE3
CSB0	AP17	DDR1_CS_N0	DDR1_CS_N0
CSB1	AN15	DDR1_CS_N1	DDR1_CS_N1
CSB2	AN17	DDR1_CS_N2	DDR1_CS_N2
CSB3	AL15	DDR1_CS_N3	DDR1_CS_N3
DCLKB0	AM20	DDR1_CLK_P0	DDR1_CLK_P0
DCLKB0	AM21	DDR1_CLK_N0	DDR1_CLK_N0
DCLKB1	AP22	DDR1_CLK_P1	DDR1_CLK_P1
DCLKB1	AP21	DDR1_CLK_N1	DDR1_CLK_N1
DCLKB2	AN20	DDR1_CLK_P2	DDR1_CLK_P2
DCLKB2	AN21	DDR1_CLK_N2	DDR1_CLK_N2
DCLKB3	AP19	DDR1_CLK_P3	DDR1_CLK_P3
DCLKB3	AP20	DDR1_CLK_N3	DDR1_CLK_N3
SCASB	AP16	DDR1_CAS*	DDR1_CAS*
SRASB	AM18	RSVD	RSVD
SWEB	AK16	DDR1_RAS*	DDR1_RAS*
SWEB	AK16	DDR1_WE*	DDR1_WE*
VREF_DQA	AB39	DDR_VREF_DQ0	DDR_VREF_DQ0
VREF_DQB	AB40	DDR_VREF_DQ1	DDR_VREF_DQ1



HASWELL[10SC1-F01150-01R]

LGA1150

(CR)

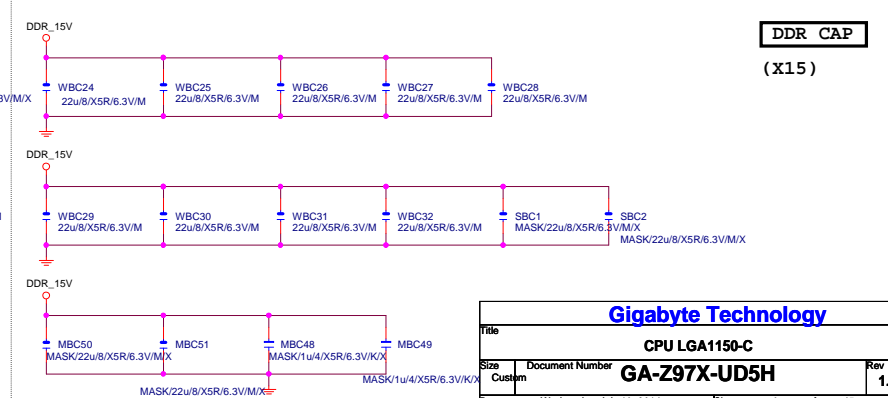
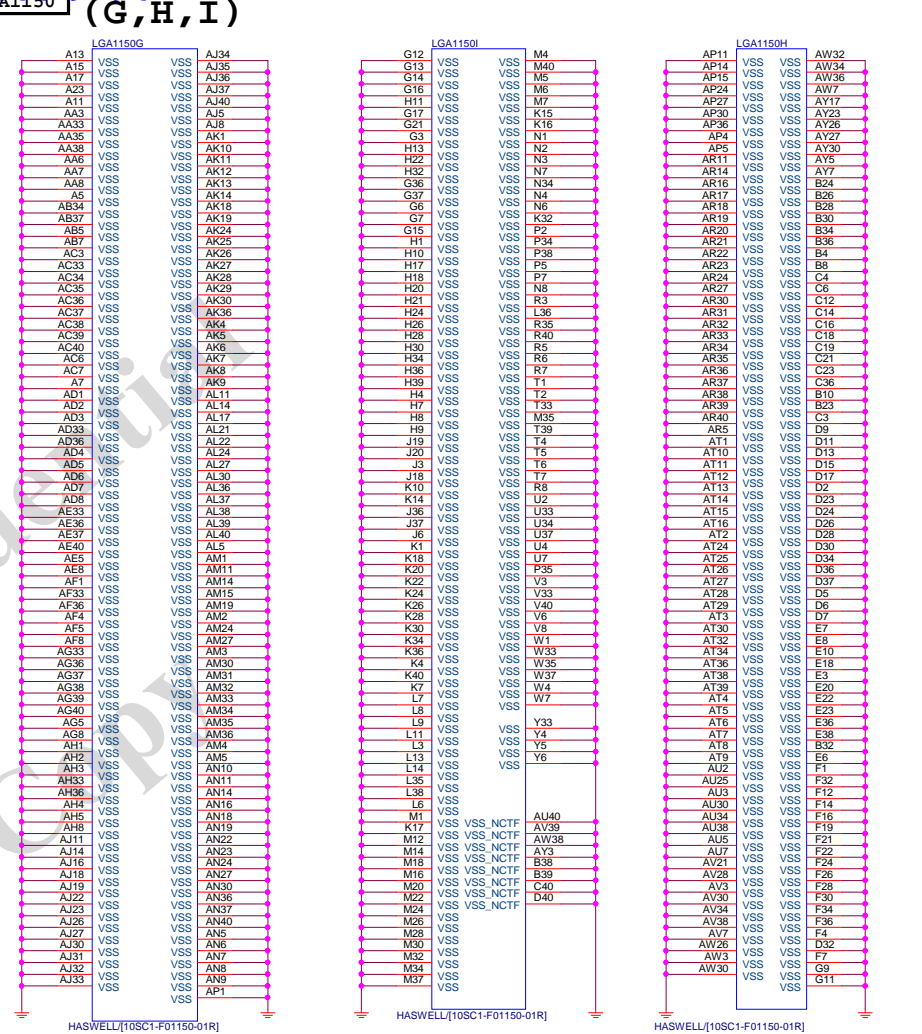
LGA1150  
ILM\_BP\_CR/115X/BKNI[12KRC-0F0001-61R]

DDR BUS

(7) MODT_A[0..3]	MODT_A[0..3]
(8) MODT_B[0..3]	MODT_B[0..3]
(7) MDA[0..63]	MDA[0..63]
(8) MDB[0..63]	MDB[0..63]
(7) DQSA[0..7]	DQSA[0..7]
(7) DQSA[0..7]	-DQSA[0..7]
(7) MAA[0..15]	MAA[0..15]
(8) MAAB[0..15]	MAAB[0..15]
(8) DQSB[0..7]	DQSB[0..7]
(8) -DQSB[0..7]	-DQSB[0..7]

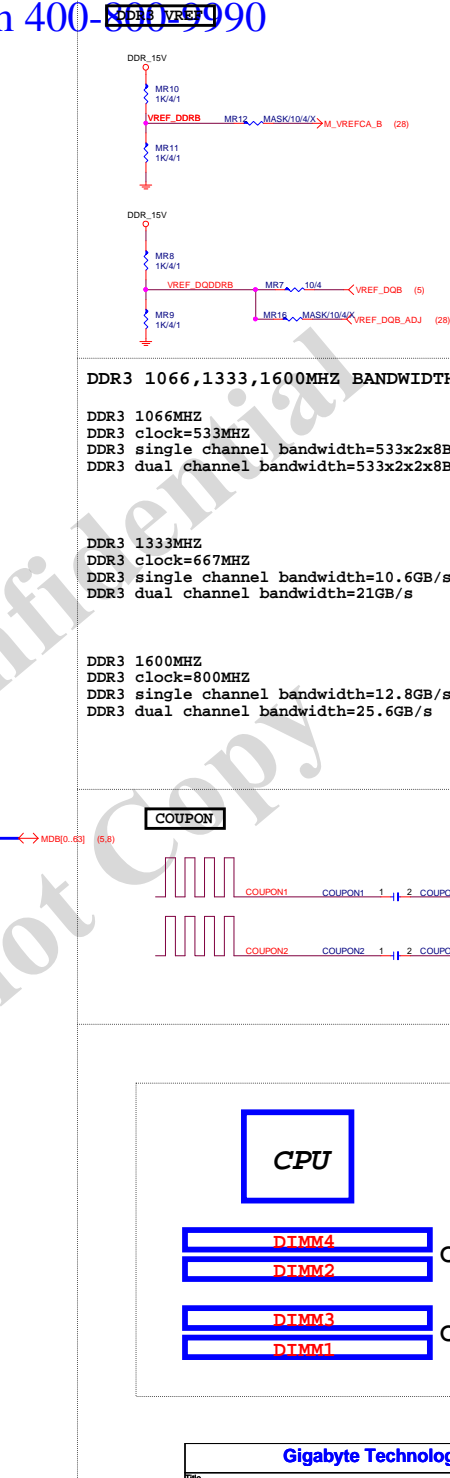
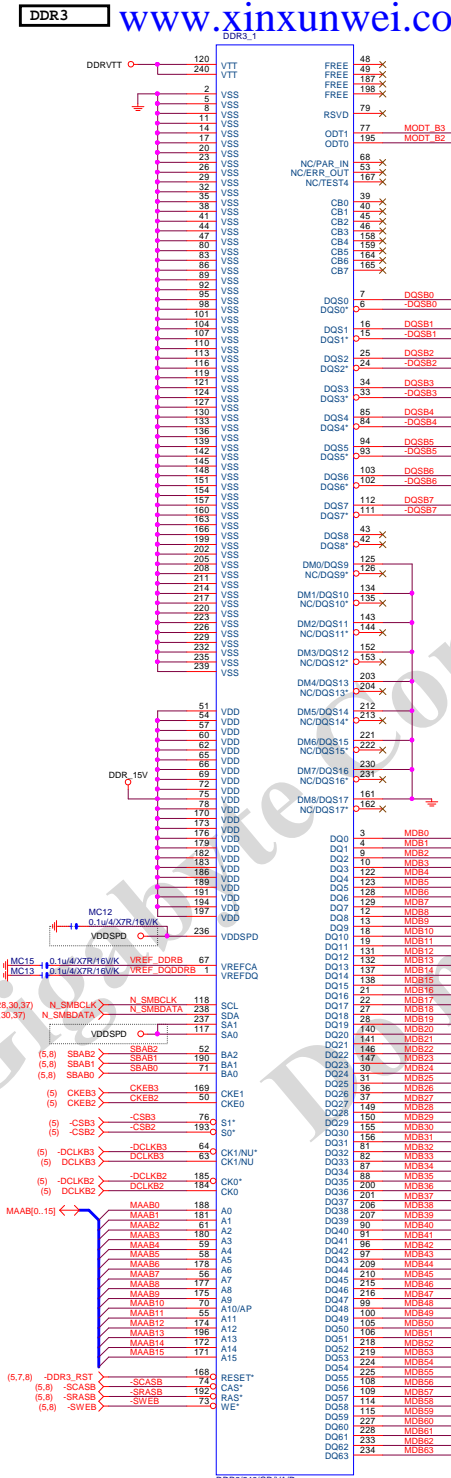
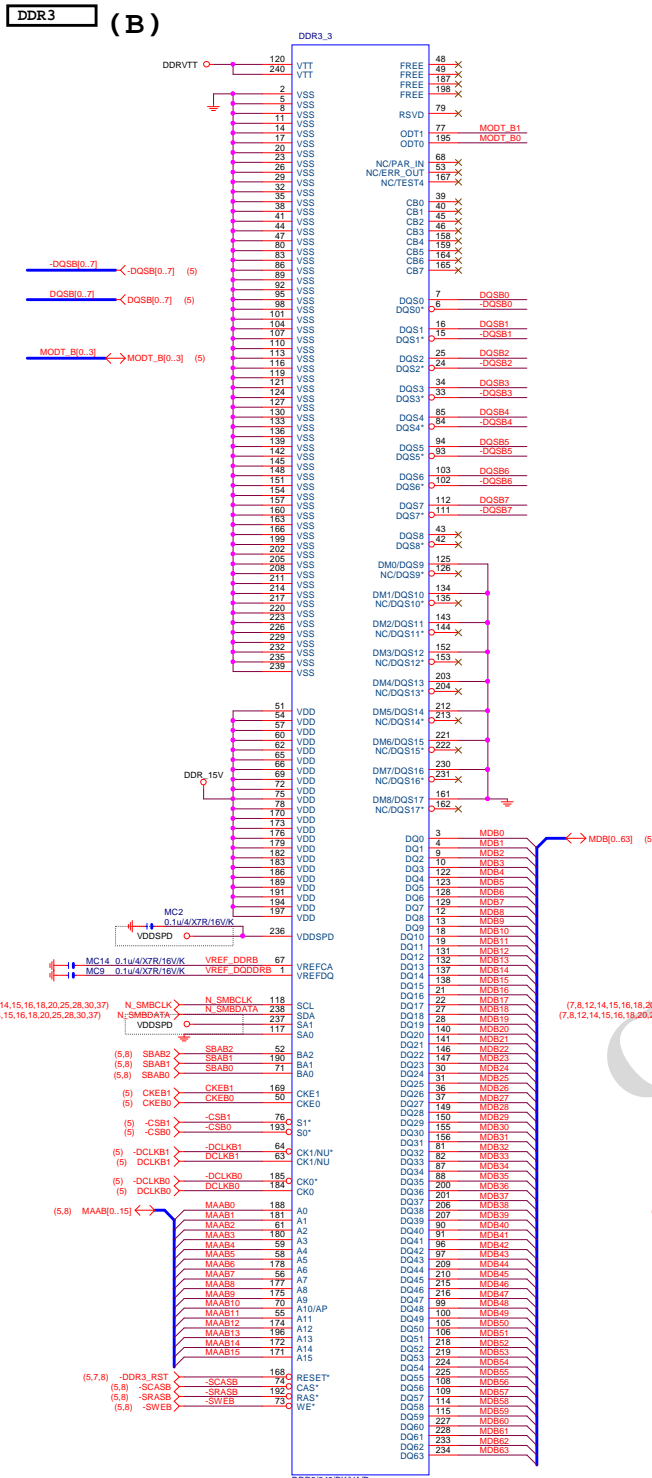
Gigabyte Technology

Title			CPU LGA1150-B
Size	Document Number	GA-Z97X-UD5H	
Custom			Rev 1.1
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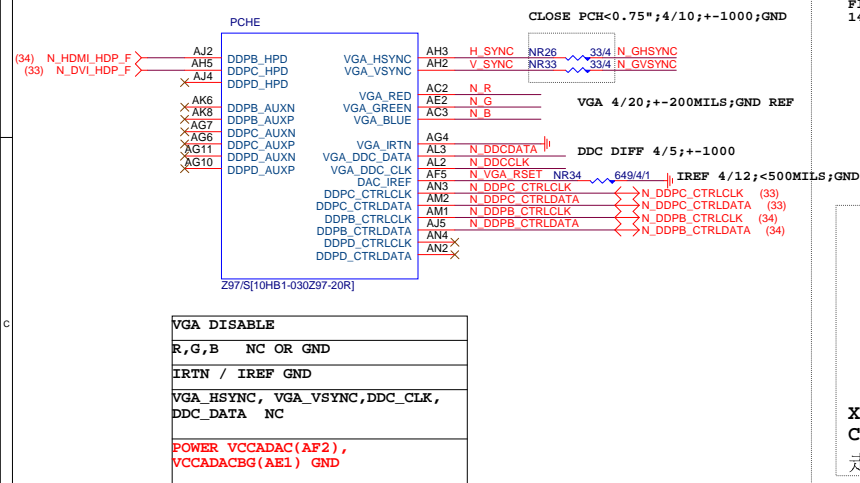






Size Custom	Document Number <b>GA-Z97X-UD5H</b>	Rev 1.11
Date: Wednesday, July 16, 2014	Sheet 9 of 45	

**PCH (E)**



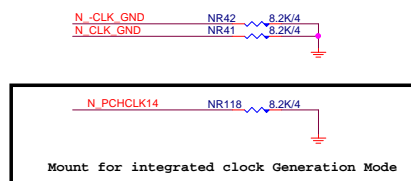
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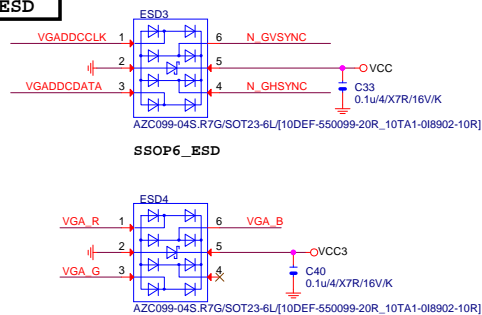
PCIEX4 CLOCK(PE\_SRCCLK\_3GIO1)由PIN R6,R7  
換成PIN W7,W6 避免跟CRYSTAL 25MHZ干擾

Differential Clock:18/4/6/4/18  
Impedance=90 +- 15%

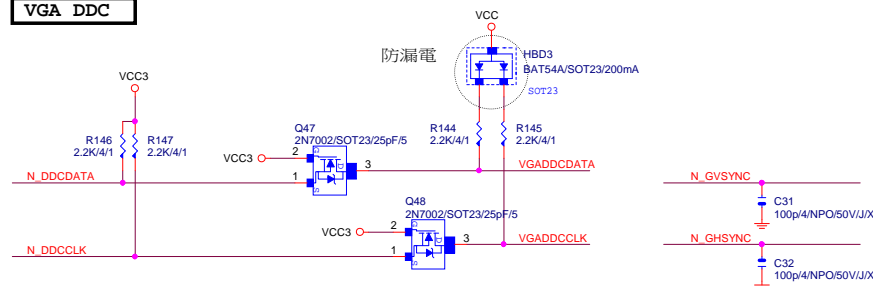
PCH CLK PD
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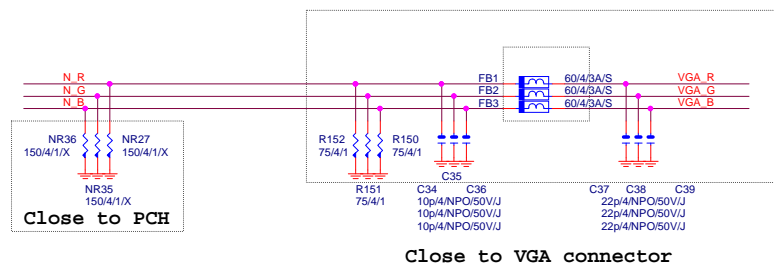
## VGA ESD



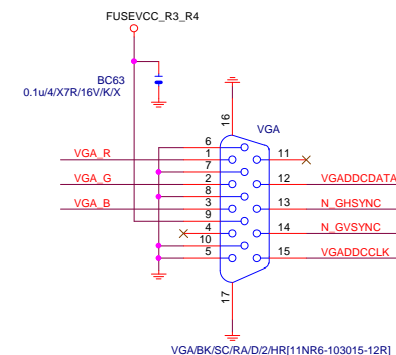
## VGA DDC



## VGA DDC



## VGA CONNECTOR

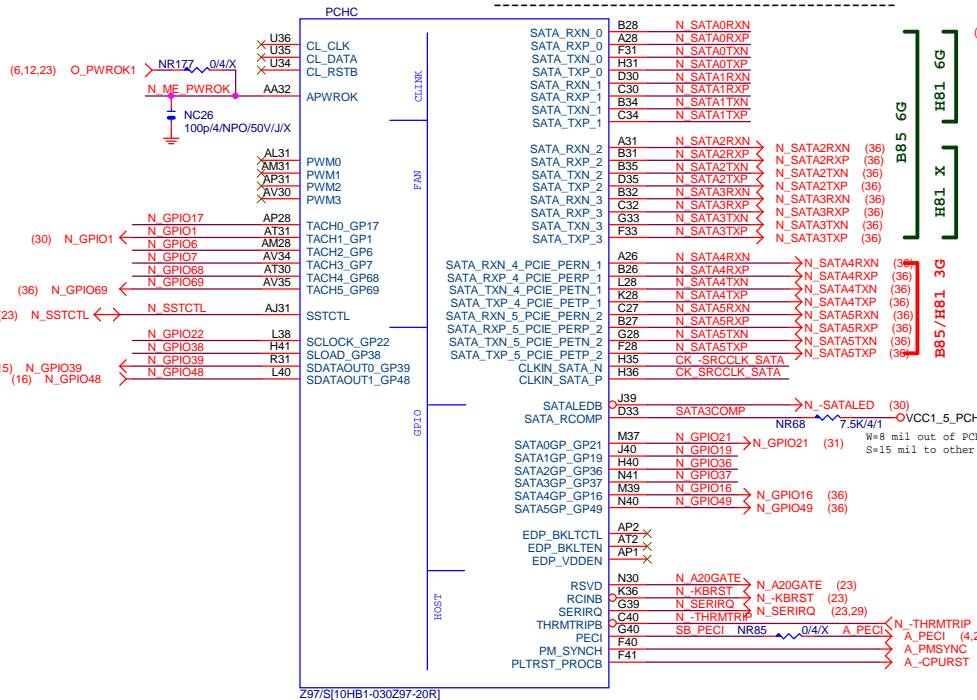


## Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number		Rev
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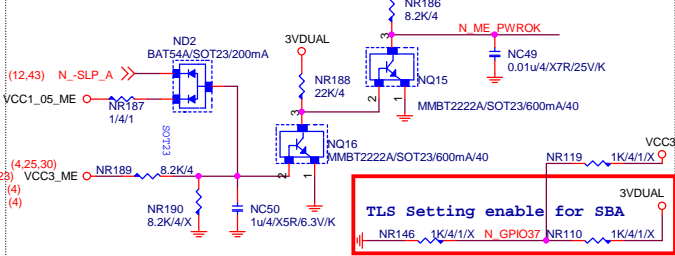
# PCH (C)

SATA3 : 20/4/4/4/20 (breakout pin 1/4/1/4)  
Impedance=85 +- 17.5%  
SATA2 4/4/4//15  
SATA3 4/4/4//20

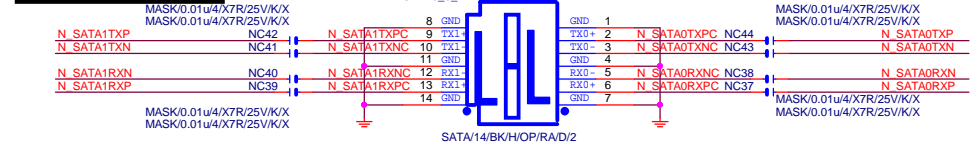


Default int pull up on GP51,  
Default SPI boot devices

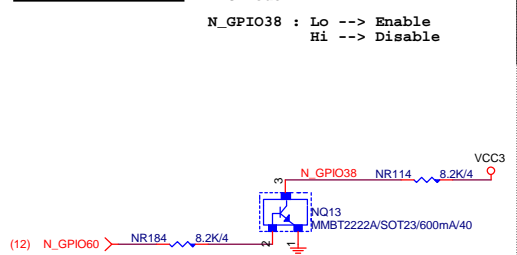
## ME PWROK



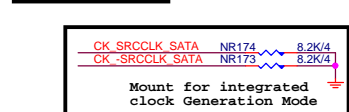
## SATA CONNECTOR



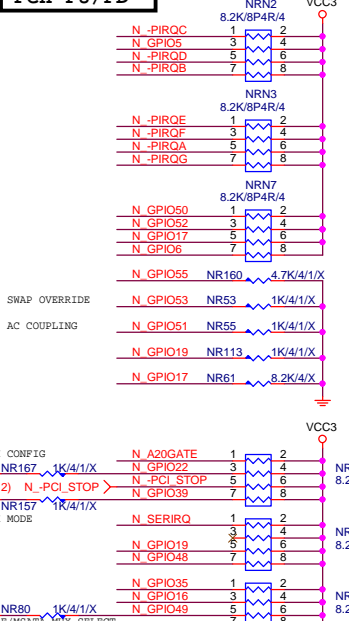
## GPIO38 Ctrl



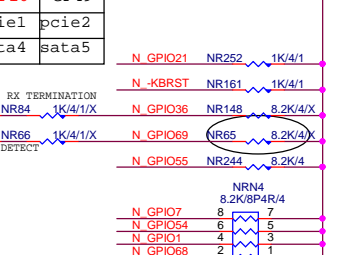
## PCH CLK PD



## PCH PU/PD



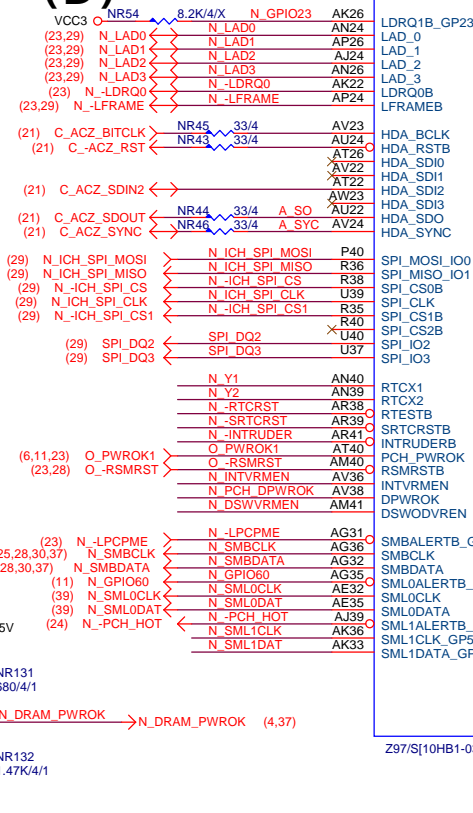
## soft strap



## Gigabyte Technology

Title			PCH HOST , SATA, PCI		
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PCHD



(23) DS\_ME DS\_ME

N\_GPIO57

NR64 8.2K/4

NR70 8.2K/4

NR140 8.2K/4

NR64 8.2K/4

NQ14 PMBT2907A/SOT23-600mA/50 SOT23

3VDUAL\_PCH

C\_ACZ\_SDOU

N\_PCH\_DPWROK (23,28)

For IT8620 Ctrl

NX2-SHT  
SHW/D0.64\*5.08\*6.74

N Y1  
N Y2

NR75 10M/4 NX2

32.768K/12.5p/20ppm/TF38/35K/D

NC16 18P4/NPO/50V/J NC18 18P4/NPO/50V/J

**BATTERY**  
CR2032

3V

2 1 N\_VBATT

BAT  
BAT-S/BK/P/S/D/S/N

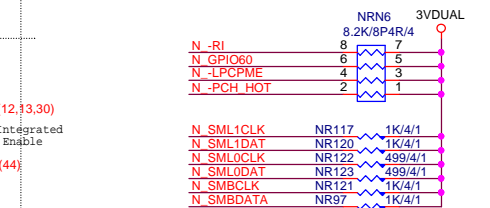
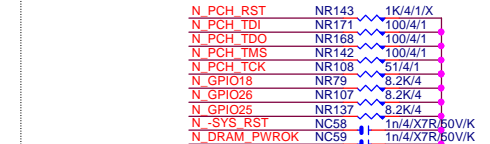
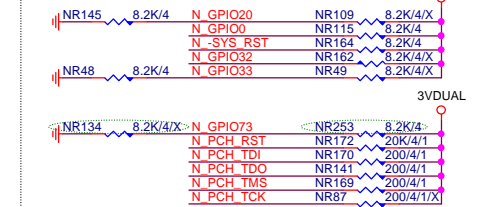
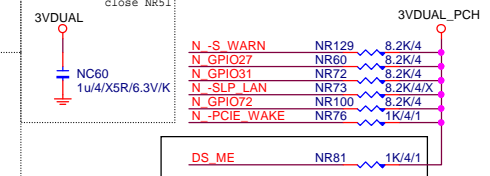
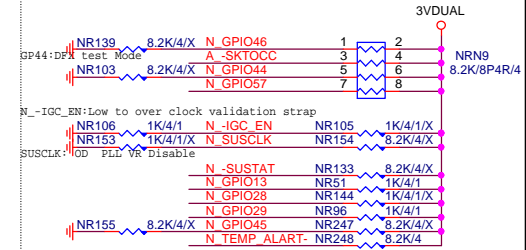
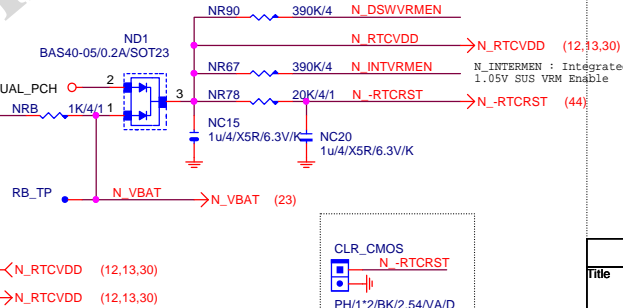
**BATTERY-DUAL-4**

**RB 必須放在-BAT外**

N\_INTRUDER NR74 1M/4

N\_SRTCST NR77 20K/4

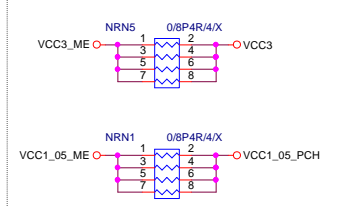
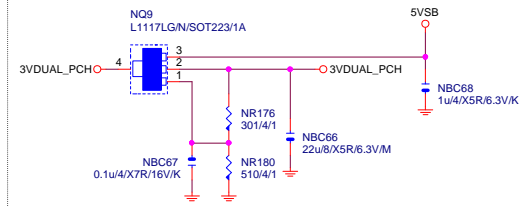
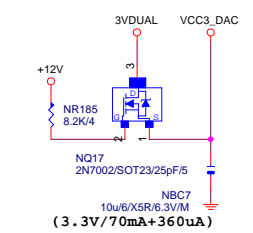
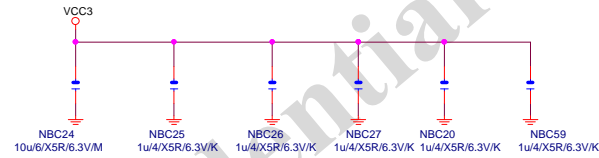
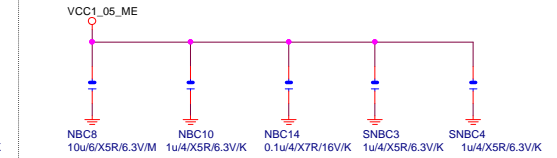
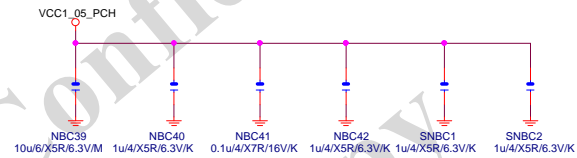
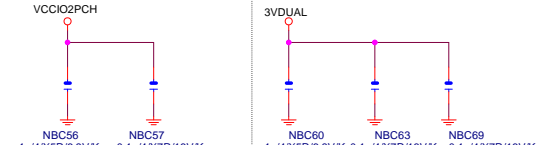
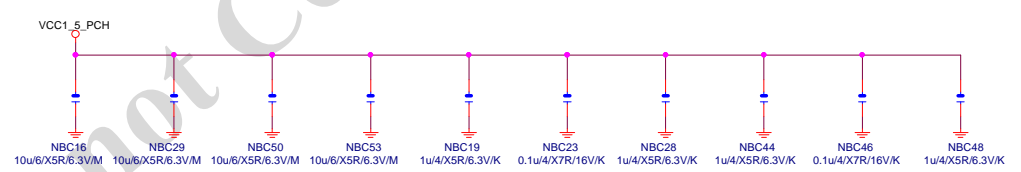
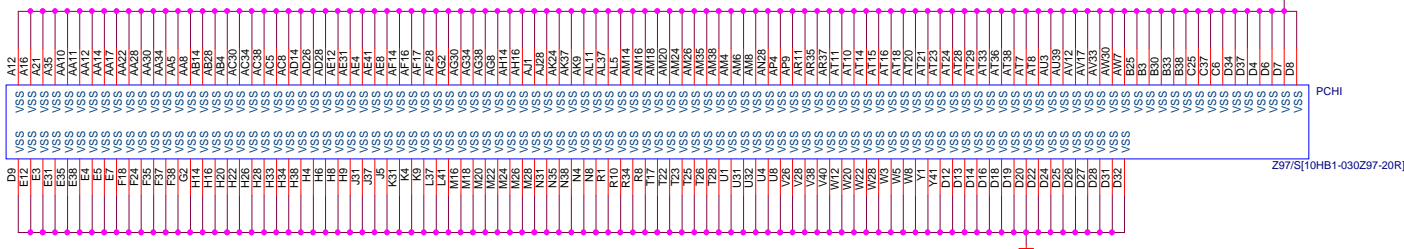
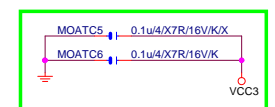
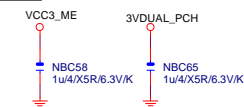
NC19  
1u4/X5R/6.3V/K



Size Custom	Document Number <b>GA-Z97X-UD5H</b>	Rev 1.11
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**PCH (H)****VCC3\_DAC****3VDUAL\_PCH****SHT\_PWR**

CLOSE北橋(注意震盪水波紋)

**(3.3V) (X6)****(1.05V) (X5)****(1.05V) (X6)****(1.05V)(X2) (3.3V) (X3)****(1.5V) (X10)****PCH (I)****CAP**

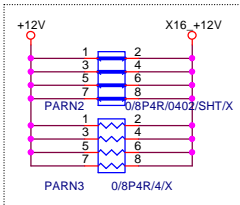
Gigabyte Technology			
Title			
PCH PWR ,GND			
Size			
Customer			
Document Number			
GA-Z97X-UD5H			
Date			
Wednesday, July 16, 2014			
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Rev			
1.1			



+12 protect  
short-wire test

PCIEX16:16/5/5/16

PA\_EXP\_RXP0[.15] >> PA\_EXP\_RXP0[.15] (4,17)  
PA\_EXP\_RXN0[.15] >> PA\_EXP\_RXN0[.15] (4,17)  
PA\_EXP\_TXP0[.15] >> PA\_EXP\_TXP0[.15] (4,17)  
PA\_EXP\_TXN0[.15] >> PA\_EXP\_TXN0[.15] (4,17)



PA_EXP_TXP0	PAC5	0.22u/4/X5R6.3V/K	PA_EXP_TXP0 C
PA_EXP_TXN0	PAC6	0.22u/4/X5R6.3V/K	PA_EXP_TXN0 C
PA_EXP_TXP1	PAC7	0.22u/4/X5R6.3V/K	PA_EXP_TXP1 C
PA_EXP_TXN1	PAC8	0.22u/4/X5R6.3V/K	PA_EXP_TXN1 C
PA_EXP_TXP2	PAC9	0.22u/4/X5R6.3V/K	PA_EXP_TXP2 C
PA_EXP_TXN2	PAC10	0.22u/4/X5R6.3V/K	PA_EXP_TXN2 C
PA_EXP_TXP3	PAC11	0.22u/4/X5R6.3V/K	PA_EXP_TXP3 C
PA_EXP_TXN3	PAC12	0.22u/4/X5R6.3V/K	PA_EXP_TXN3 C
PA_EXP_TXP4	PAC13	0.22u/4/X5R6.3V/K	PA_EXP_TXP4 C
PA_EXP_TXN4	PAC14	0.22u/4/X5R6.3V/K	PA_EXP_TXN4 C
PA_EXP_TXP5	PAC15	0.22u/4/X5R6.3V/K	PA_EXP_TXP5 C
PA_EXP_TXN5	PAC16	0.22u/4/X5R6.3V/K	PA_EXP_TXN5 C
PA_EXP_TXP6	PAC17	0.22u/4/X5R6.3V/K	PA_EXP_TXP6 C
PA_EXP_TXN6	PAC18	0.22u/4/X5R6.3V/K	PA_EXP_TXN6 C
PA_EXP_TXP7	PAC19	0.22u/4/X5R6.3V/K	PA_EXP_TXP7 C
PA_EXP_TXN7	PAC20	0.22u/4/X5R6.3V/K	PA_EXP_TXN7 C
PA_EXP_SW_TXP8	PAC21	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP8 C
PA_EXP_SW_TXN8	PAC22	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN8 C
PA_EXP_SW_TXP9	PAC23	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP9 C
PA_EXP_SW_TXN9	PAC24	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN9 C
PA_EXP_SW_TXP10	PAC25	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP10 C
PA_EXP_SW_TXN10	PAC26	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN10 C
PA_EXP_SW_TXP11	PAC27	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP11 C
PA_EXP_SW_TXN11	PAC28	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN11 C
PA_EXP_SW_TXP12	PAC29	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP12 C
PA_EXP_SW_TXN12	PAC30	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN12 C
PA_EXP_SW_TXP13	PAC31	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP13 C
PA_EXP_SW_TXN13	PAC32	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN13 C
PA_EXP_SW_TXP14	PAC33	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP14 C
PA_EXP_SW_TXN14	PAC34	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN14 C
PA_EXP_SW_TXP15	PAC35	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXP15 C
PA_EXP_SW_TXN15	PAC36	0.22u/4/X5R6.3V/K	PA_EXP_SW_TXN15 C

PA\_EXP\_SW\_RXP8[.15] >> PA\_EXP\_SW\_RXP8[.15] (17)  
PA\_EXP\_SW\_RXN8[.15] >> PA\_EXP\_SW\_RXN8[.15] (17)  
PA\_EXP\_SW\_TXP8[.15] >> PA\_EXP\_SW\_TXP8[.15] (17)  
PA\_EXP\_SW\_TXN8[.15] >> PA\_EXP\_SW\_TXN8[.15] (17)

PCI-E REV:1.1--> 2.5GHZ

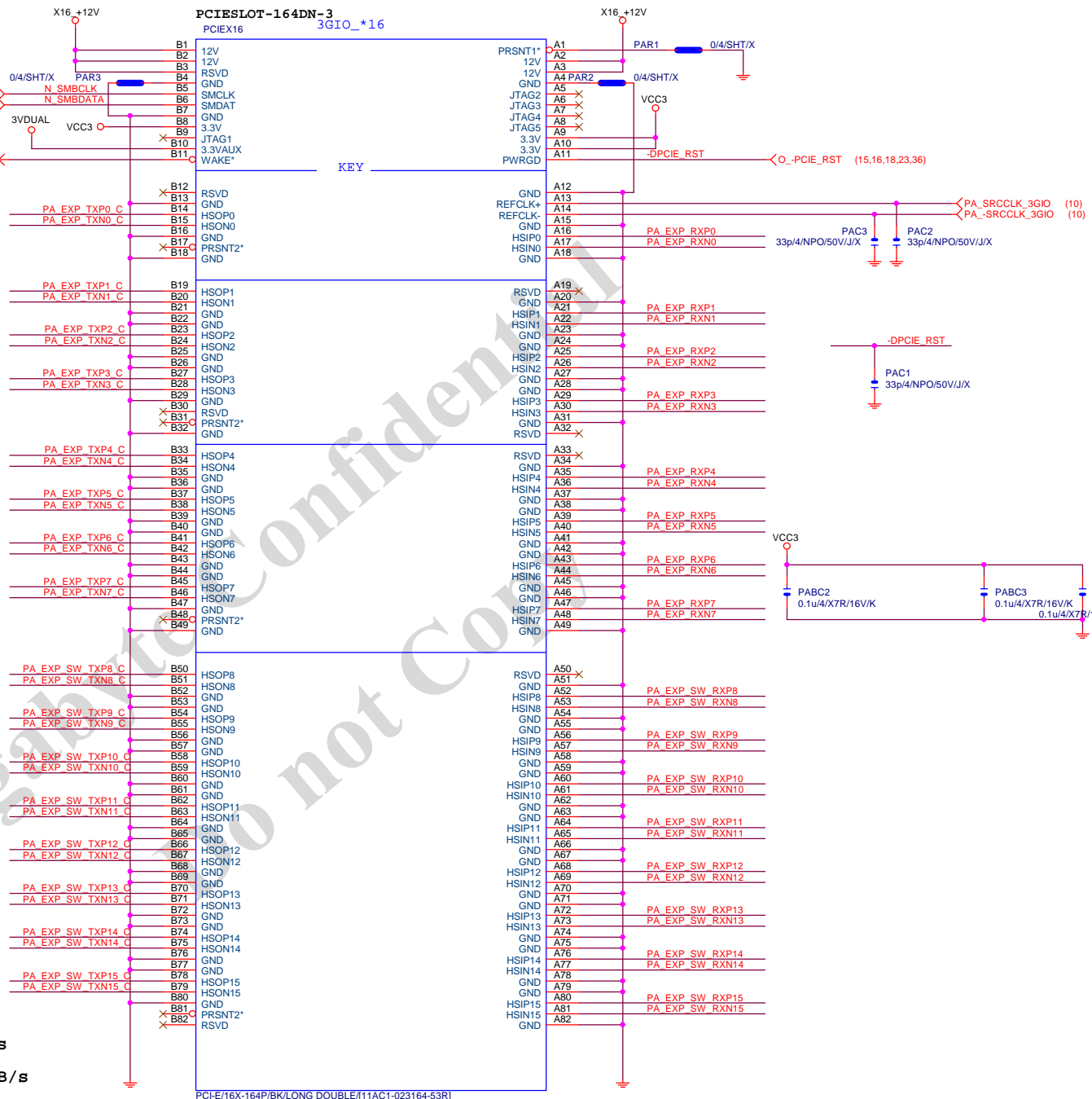
PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

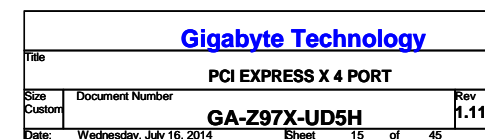
PCI-E REV:2.0--> 5GHZ

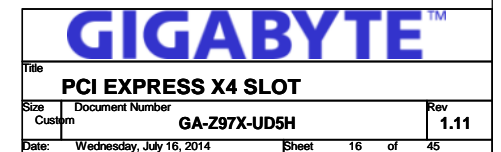


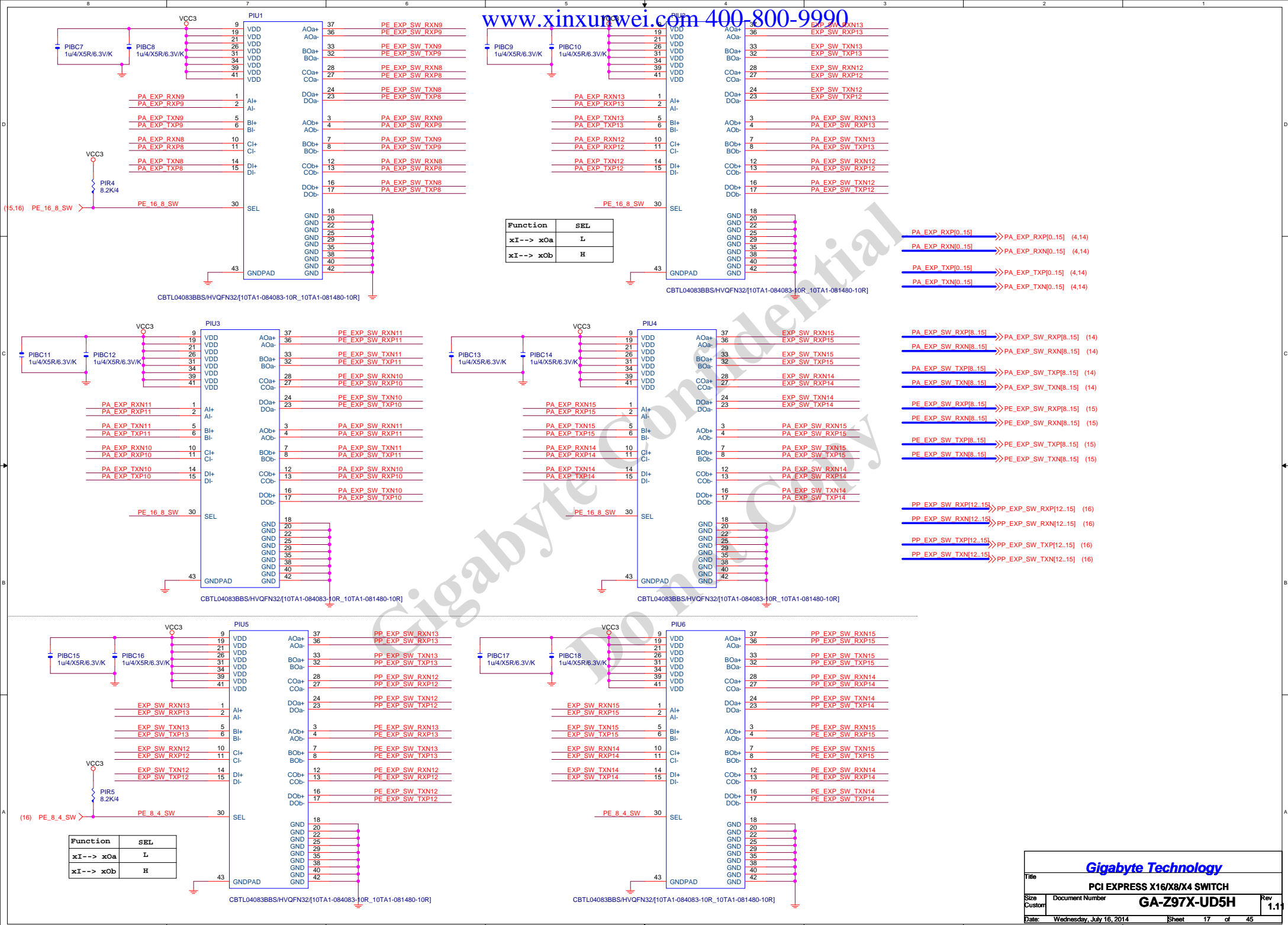
Gigabyte Technology

Title			
PCI EXPRESS * 16			
Size	Document Number		Rev
Custom	GA-Z97X-UD5H		1.11
Date:	Wednesday, July 16, 2014		Sheet 14 of 45

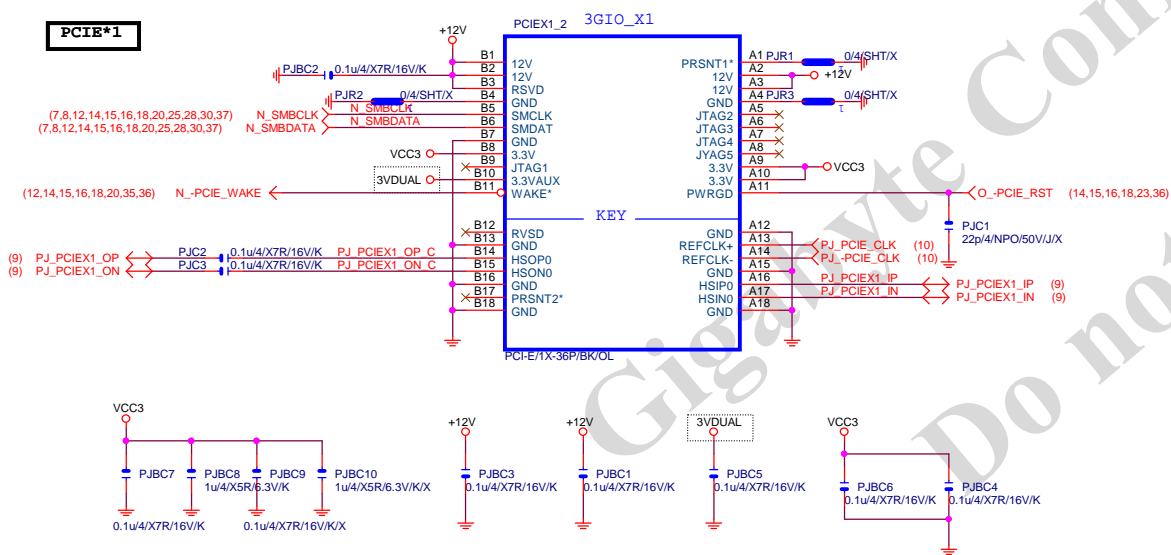
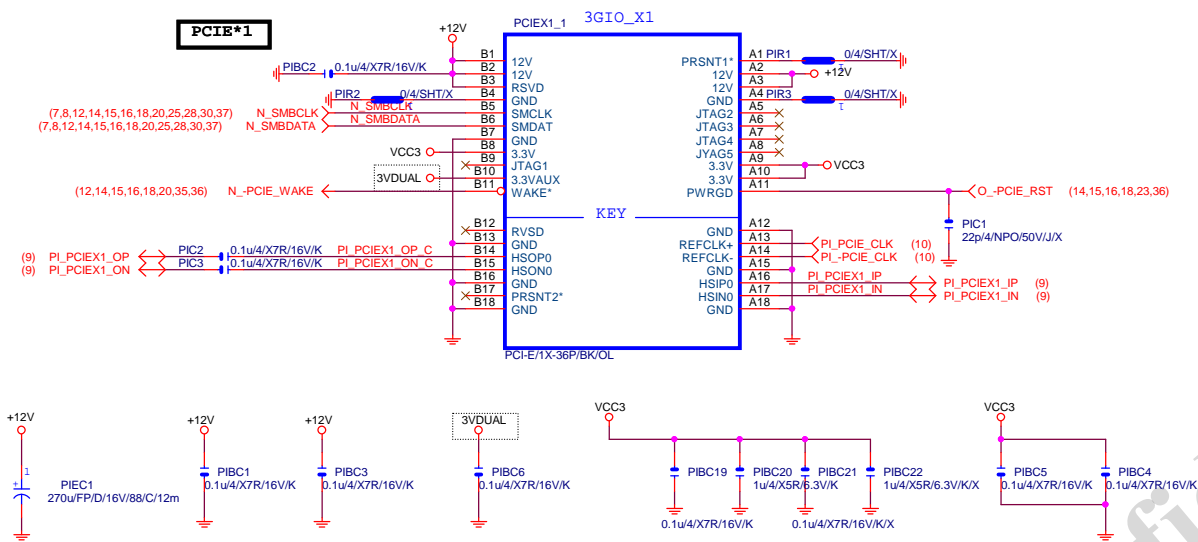


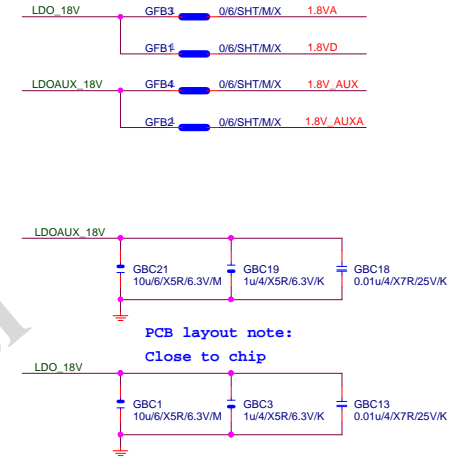
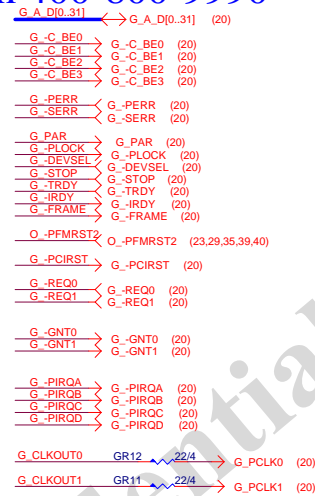
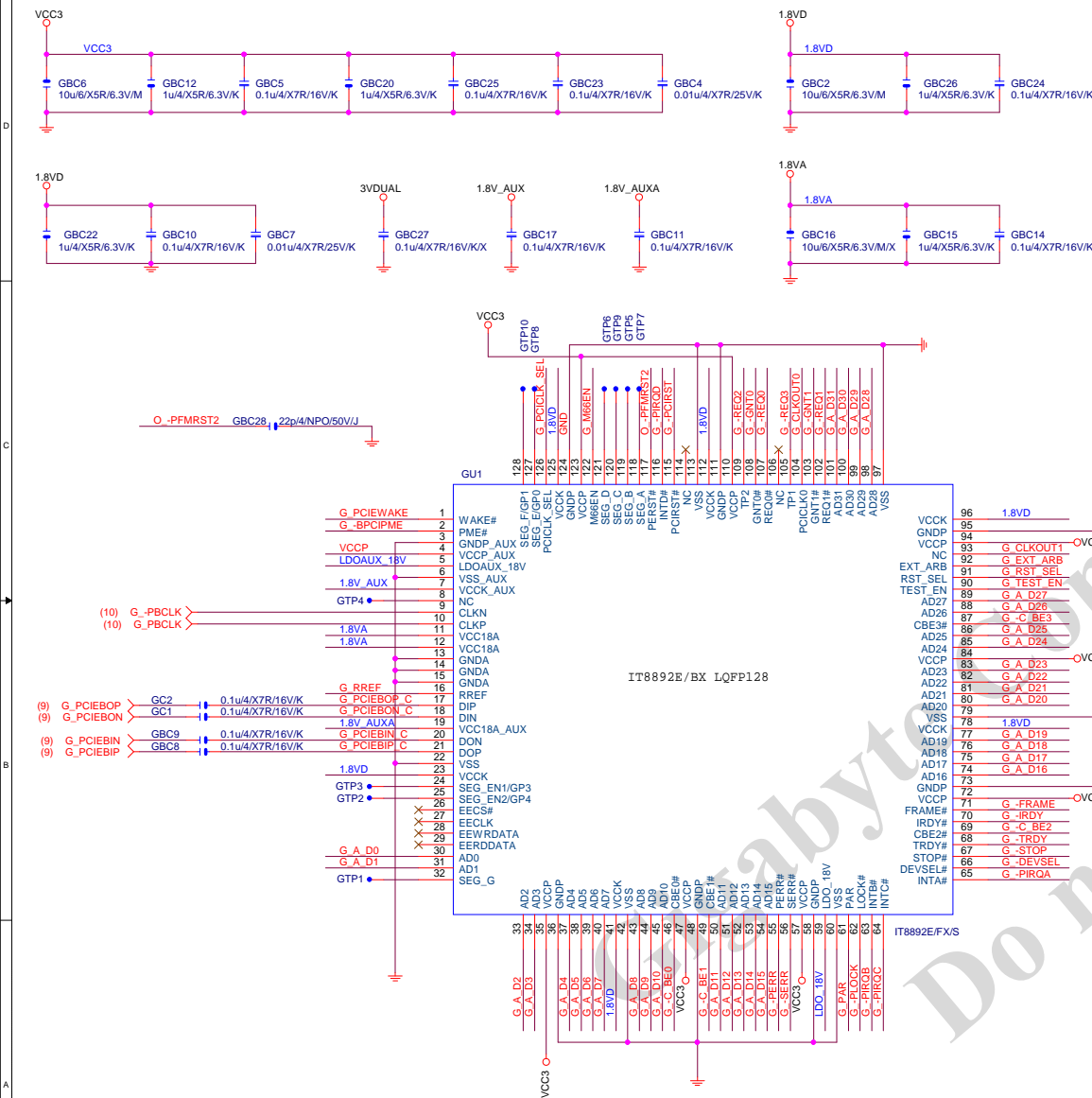




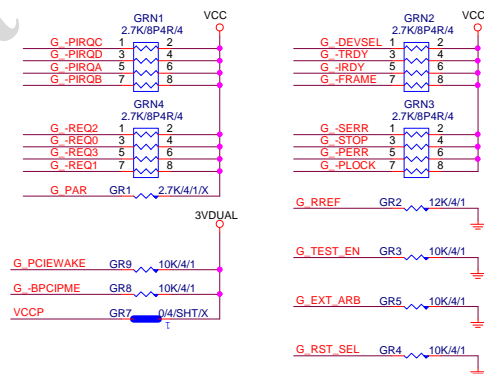
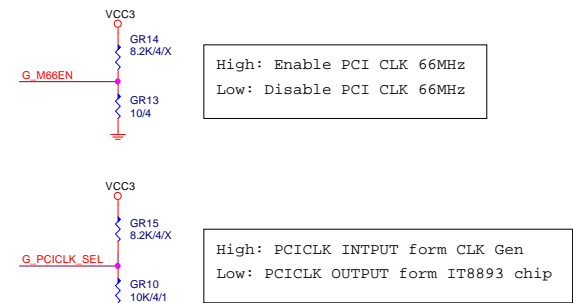


Gigabyte Technology





PCB layout note:  
Close to chip



<b>Gigabyte Technology</b>			
Title			
<b>IT8892E</b>			
Size	Document Number		Rev
Custom	<b>GA-Z97X-UD5H</b>		<b>1.11</b>
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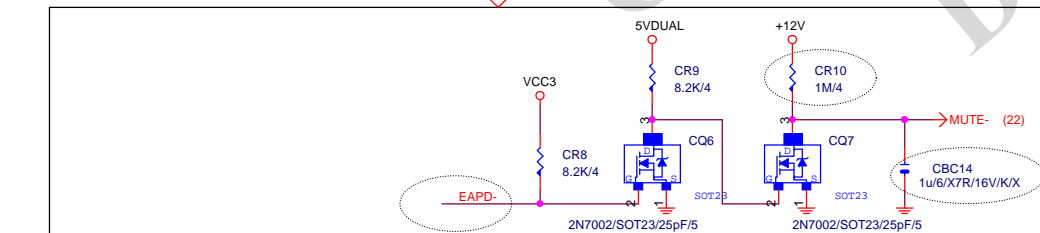
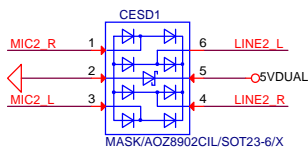
## AZALIA CODEC

Thermal pad is DGND

Digital Area

Analog Area

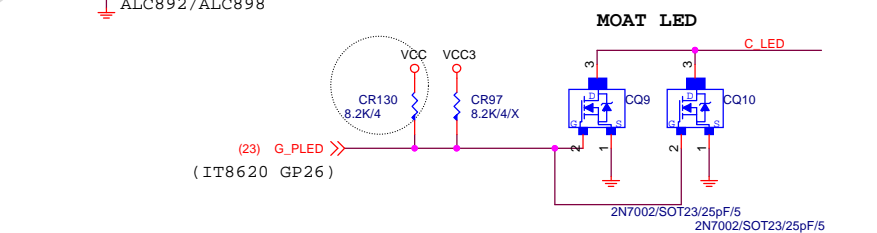
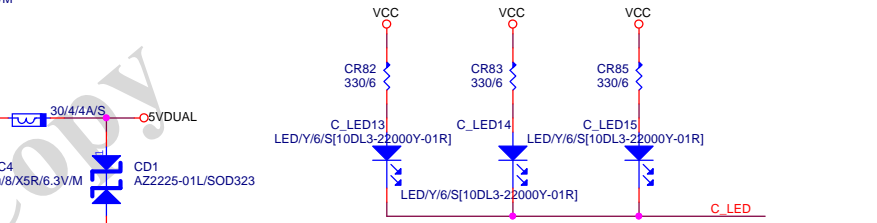
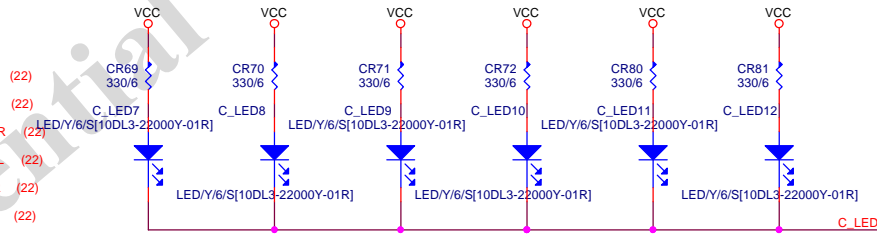
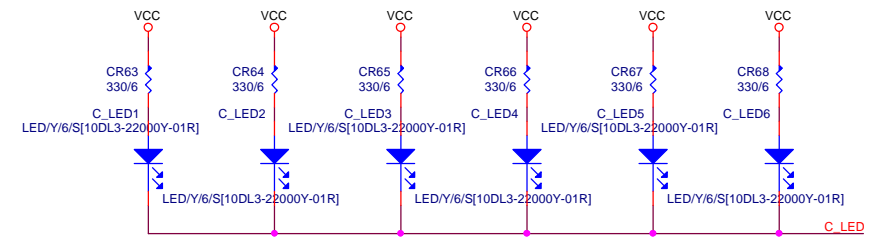
0/6/X For AGND/GND  
moat under Codec  
Body



Close to ALC1150

CU1  
ALC1150-CG/QFN48

UD5H不上金屬罩&amp;LED



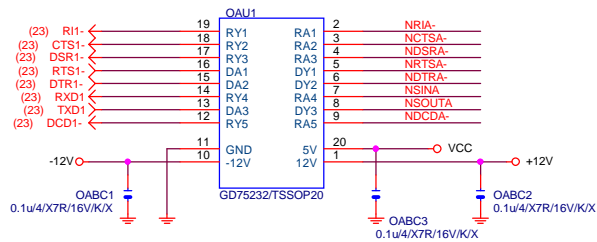
Gigabyte Technology

Title			HD AUDIO ALC887B-VD2/VT1708S/VT2021
Size	Document Number	GA-Z97X-UD5H	
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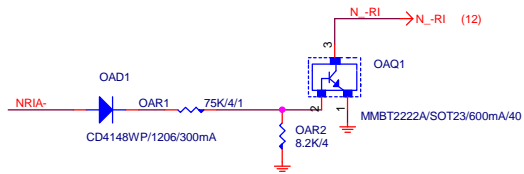




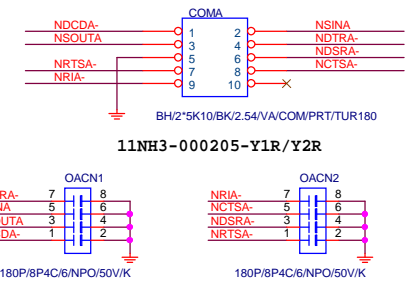
## COMA



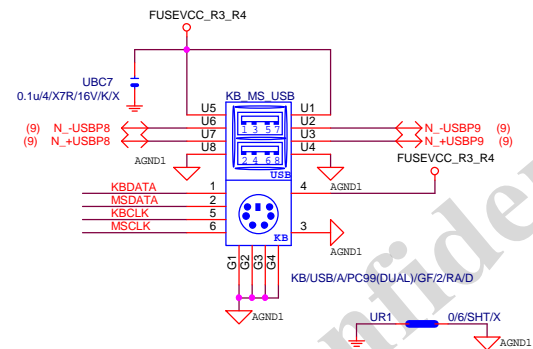
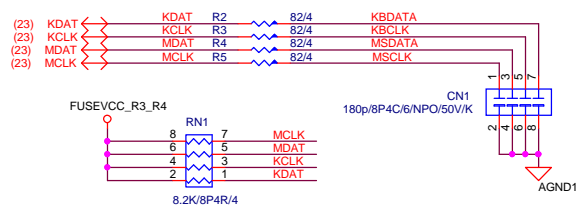
## COM RI



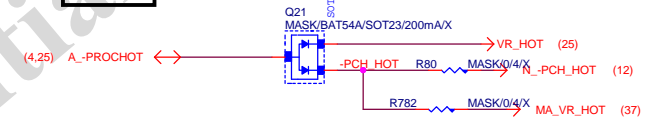
## COM BUFFER



## KB/MS/USB



## -PROHOT

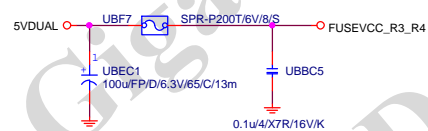


## Thunderbolt pin header

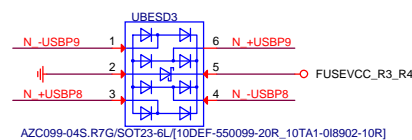
Removed

## R\_USB

## USB20 FUSE

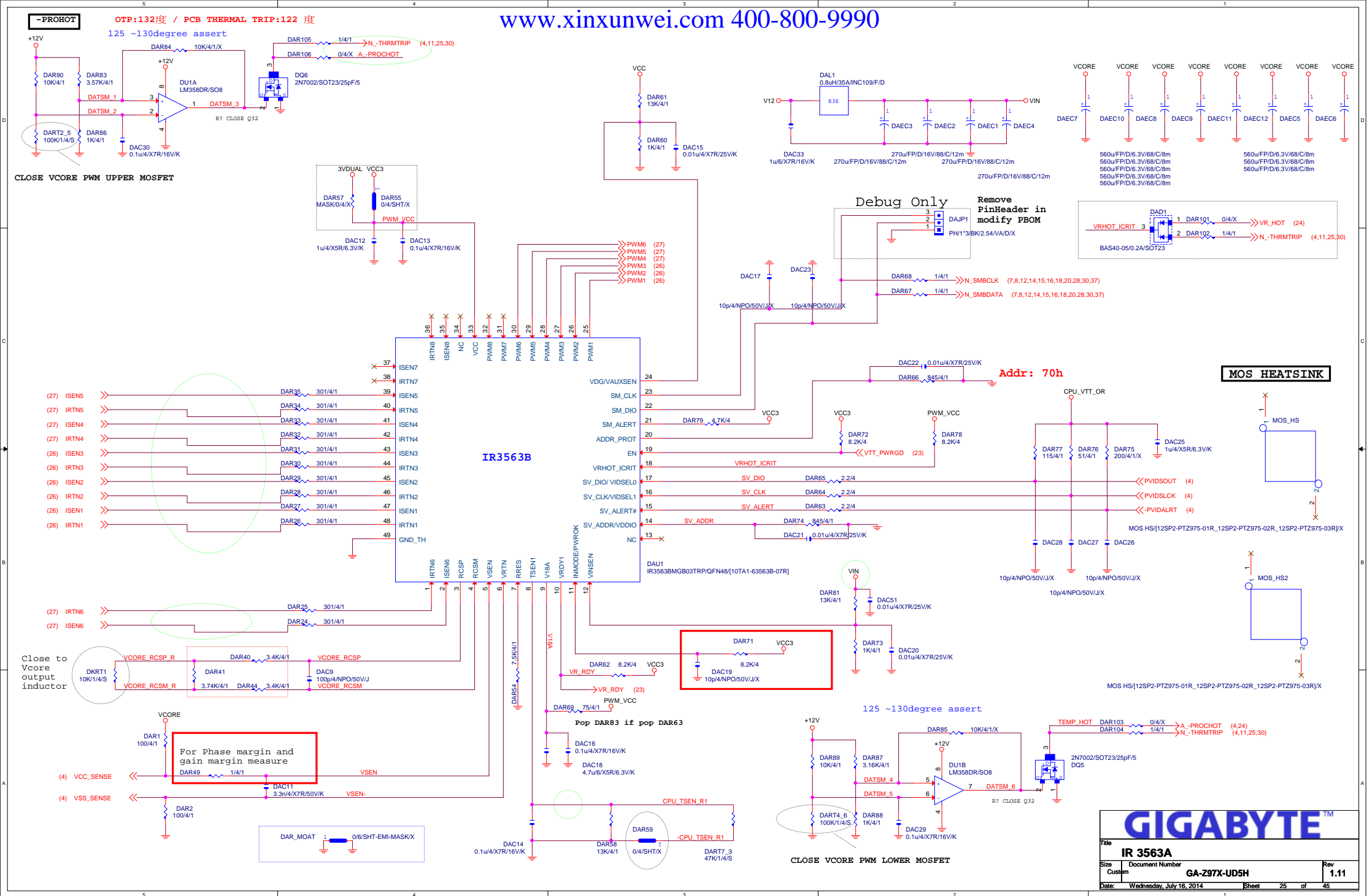


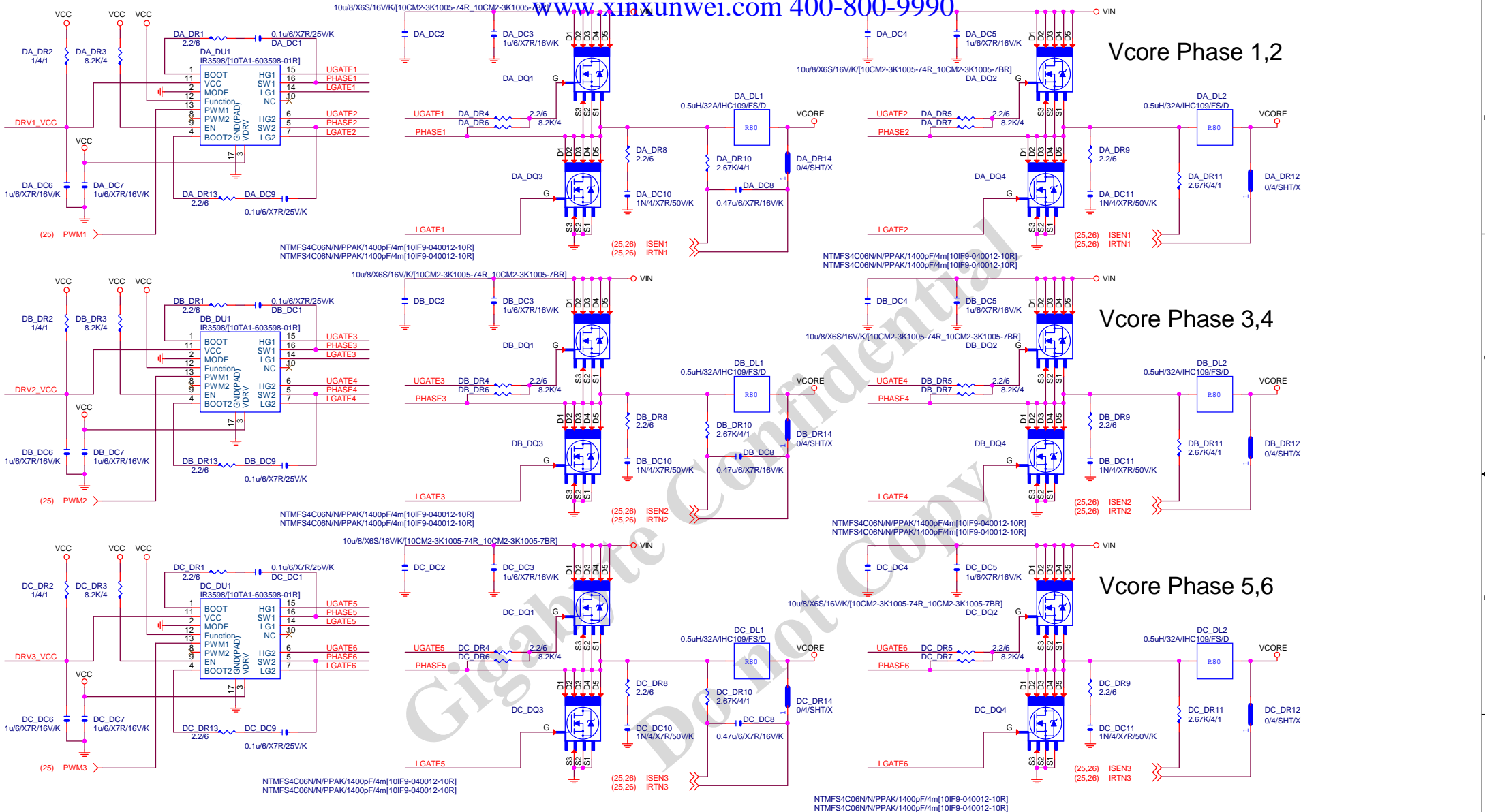
## USB20 ESD PROTECT



Gigabyte Technology

COM/ PROHOT/ R_USB			
File	Document Number	GA-Z97X-UD5H	Rev 1.11
Size	Custom		
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Vcore Phase 1,2

Vcore Phase 3,4

Vcore Phase 5,6

FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

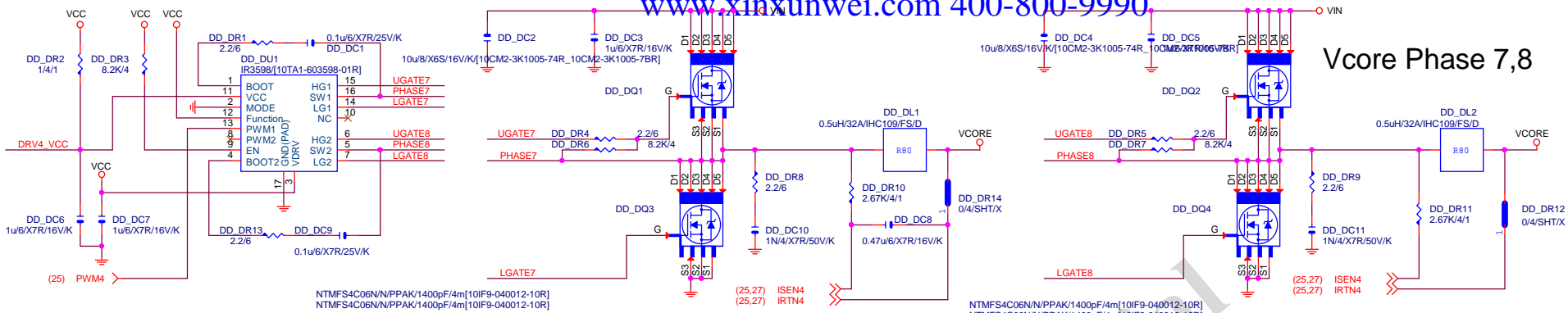
function = 0 --> Quad mode  
function = 1 --> Doubled mode

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

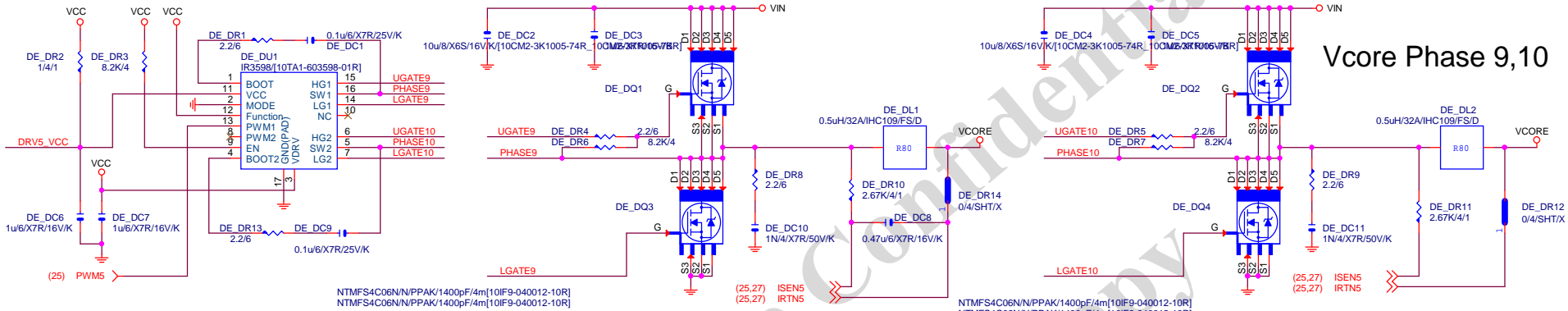
GIGABYTE TECHNOLOGY			
Title			
CPU CORE_IR3563B			
Size			
Document Number			
GA-Z97X-UD5H			
Rev			
1.11			
Date			
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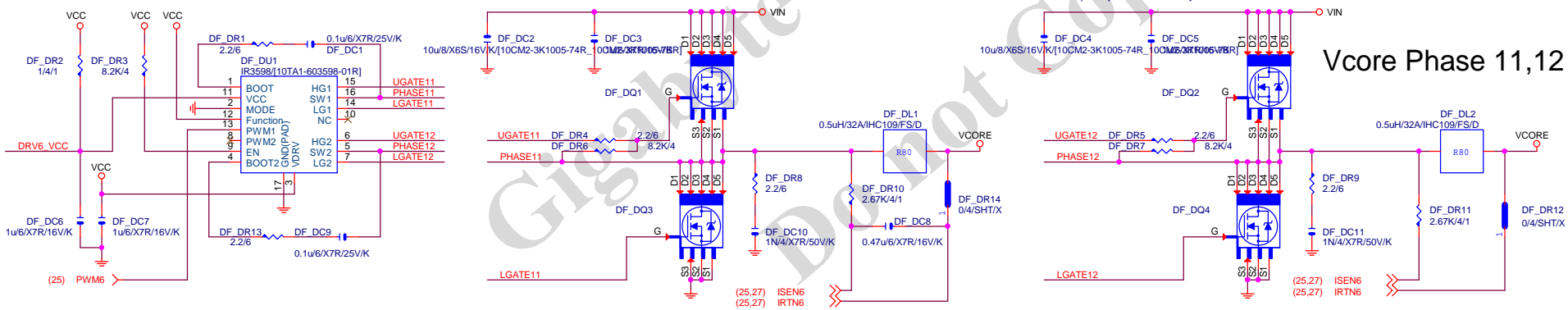
## Vcore Phase 7,8



## Vcore Phase 9,10



## Vcore Phase 11,12



FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

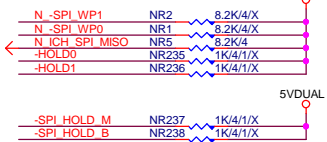
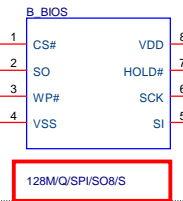
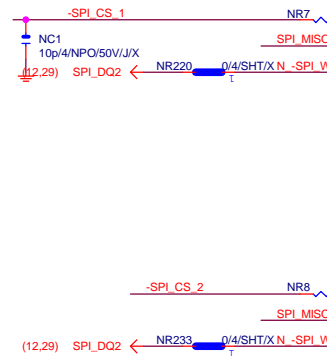
function = 0 --> Quad mode  
function = 1 --> Doubled mode

In Quad mode, IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without PU

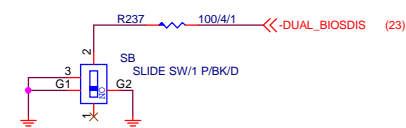
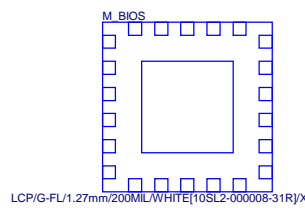
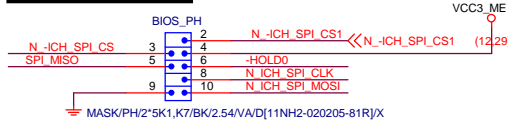
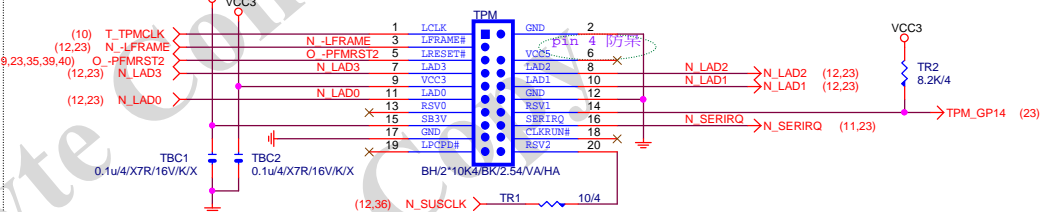
GIGABYTE TECHNOLOGY			
Title	CPU CORE_IR3563B		
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.11	
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指定用DII



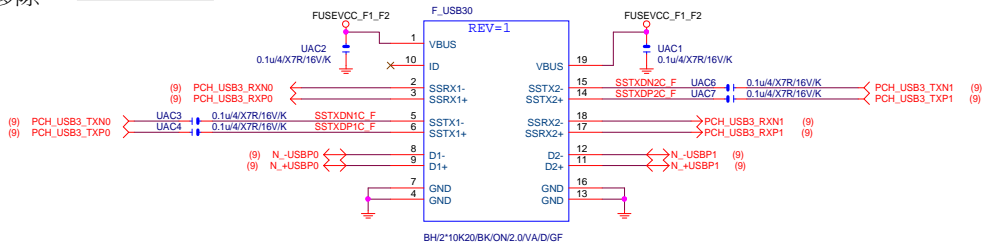
1	means	floating
0	means	PD 1K



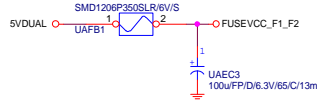
<b><i>Gigabyte Technology</i></b>			
Title		<b>DUAL BIOS, TPM</b>	
Size	Document Number	<b>GA-Z97X-UD5H</b>	Rev
Custom			<b>1.11</b>
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0.2 移除

### Front USB3.0

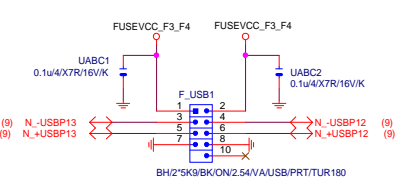


### F\_USB30 PWR

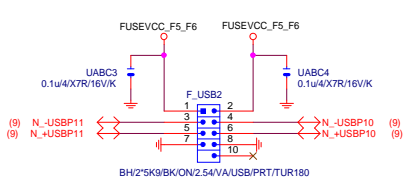


Close to connector

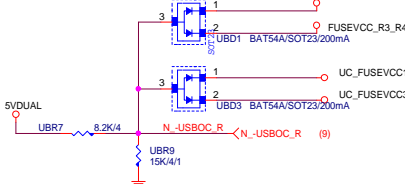
### FRONT USB1



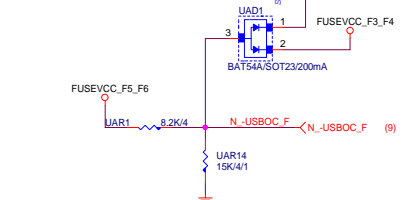
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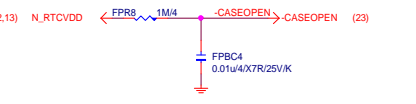
### -USBOC\_R



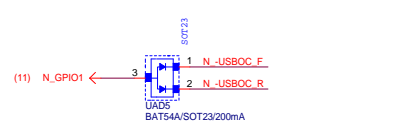
### -USBOC\_F



### CASE OPEN

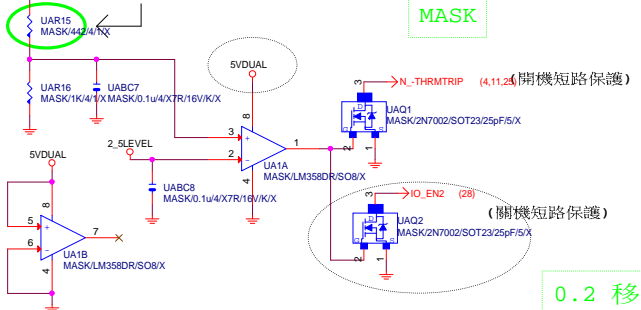


### F\_USB POWER PROTECT



### USB2.0 Signal & power short protection

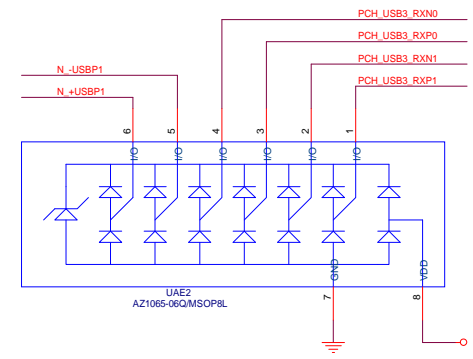
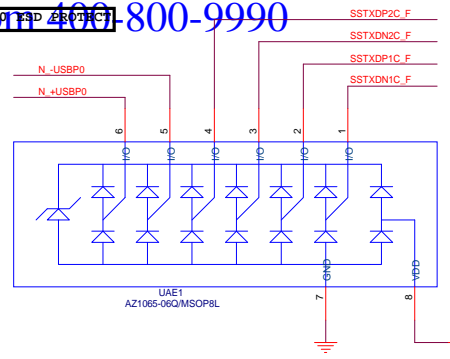
USB2.0 Signal > 4.85V  
Enable --> 3VDUAL=3.6V



MASK

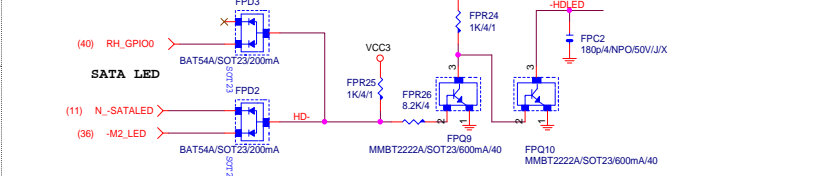
0.2 移除

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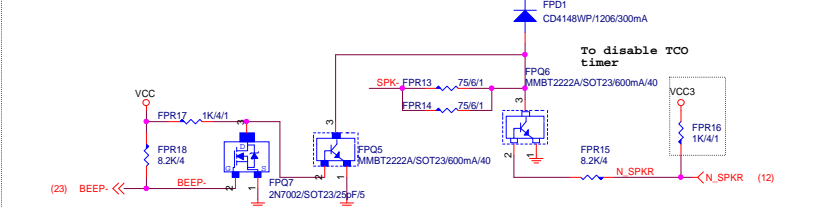


### SATA LED

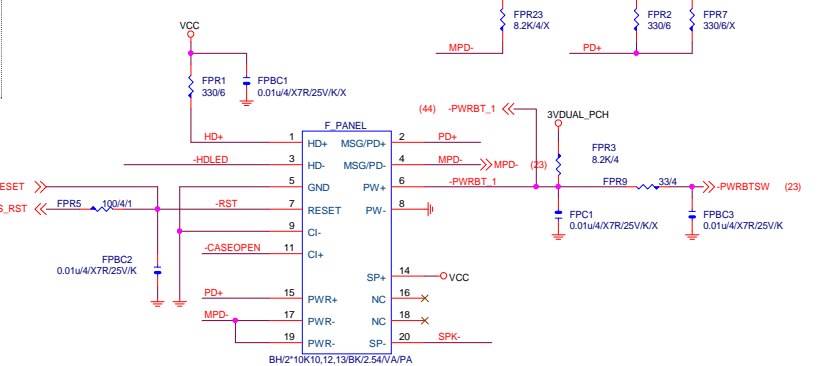
SATALED# signal open-collector, pull-up (8.2 kΩ to 10 kΩ) to Vcc3\_3



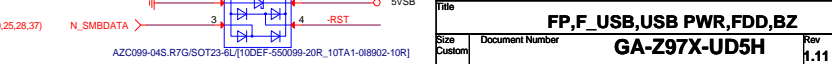
### SPKR



### INTEL FRONT PANEL



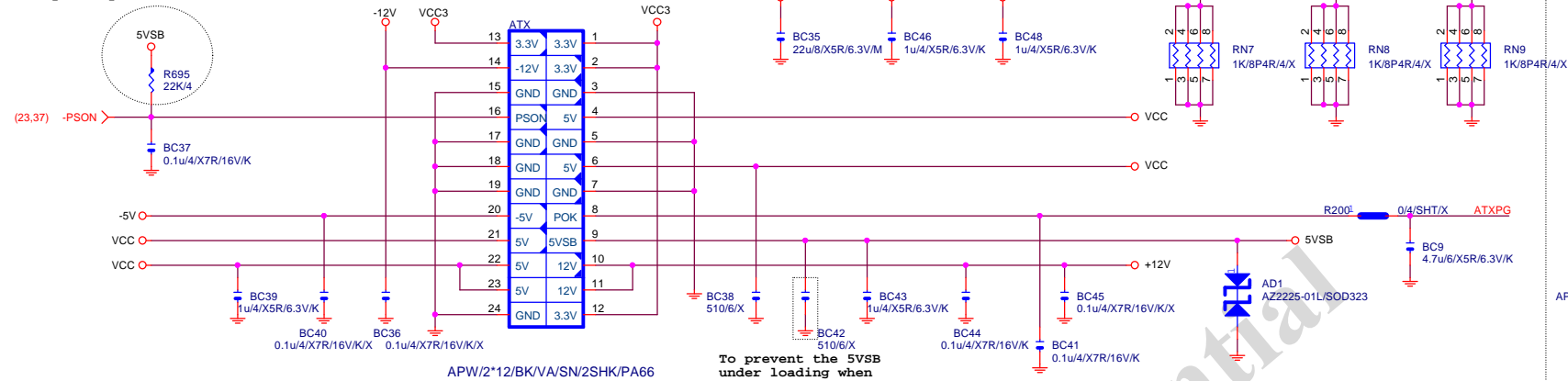
### F\_PANEL



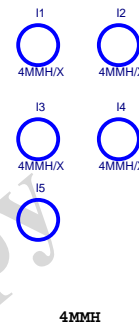
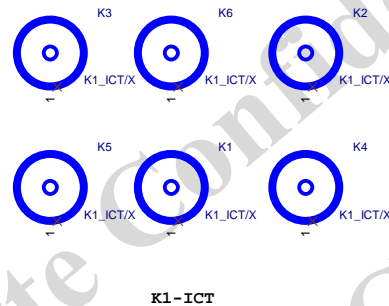
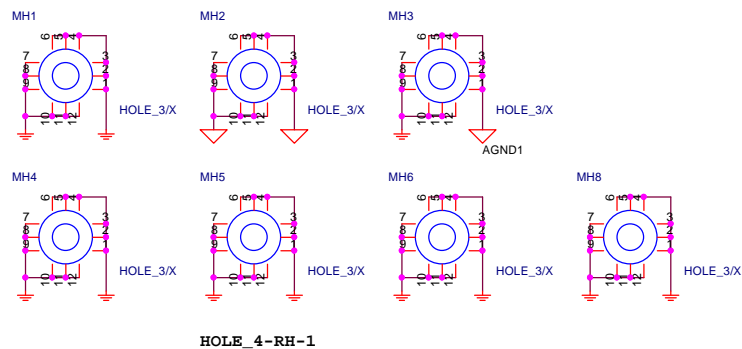
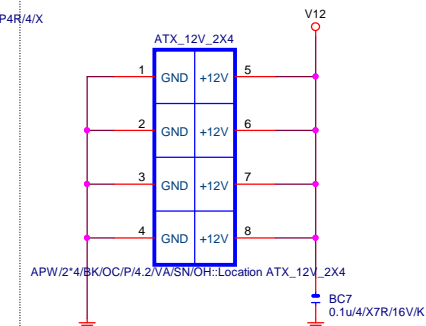
Gigabyte Technology			
FP,F_USB,USB PWR,FDD,BZ			
GA-Z97X-UD5H			
Title	Document Number	Rev	1.11
Size	Custom	Date	Wednesday, July 16, 2014
Sheet	30	of	45

## ATXX24 POWER CONNECTOR

Patch some PSU no internal pull up resistor

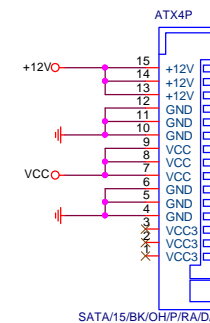
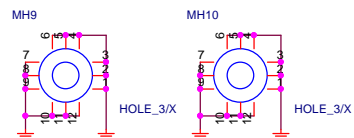
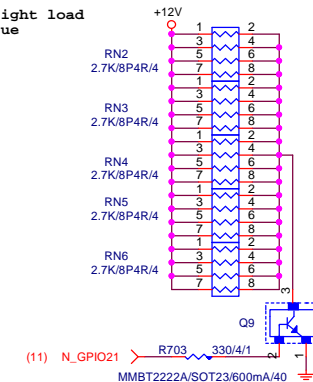


## ATXX4 POWER CONNECTOR



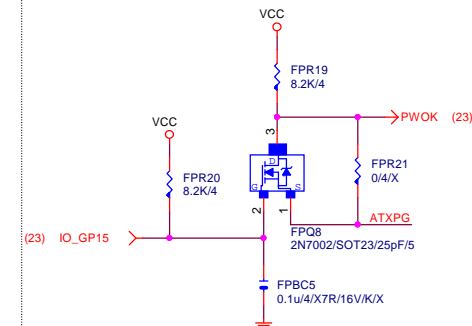
## 【技術通報R&amp;D技術通報153】

To fix 12V light load abnormal issue



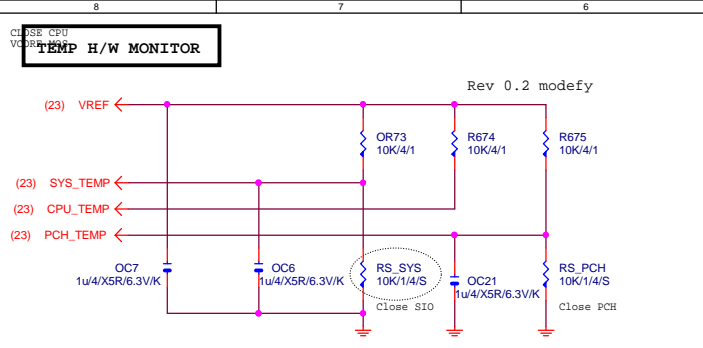
## PWOK PATCH

## 【技術通報R&amp;D技術通報154】



Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-Z97X-UD5H	1.11
Date:	Wednesday, July 16, 2014	Sheet 31 of 45

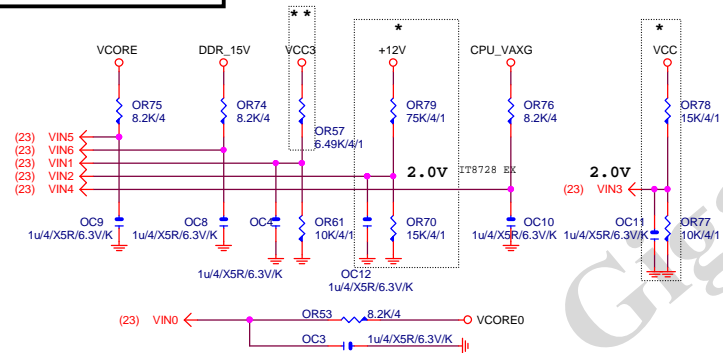


Thrmtrip#改用LM358做

# VOLTAGE-- H/W MONITOR

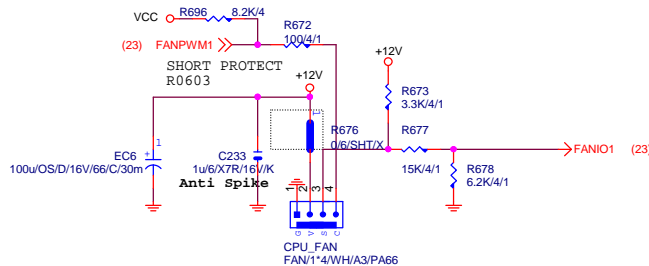
\* IT8728 BX  
\* IT8728 CX

VIN2 must +12V input  
VIN3 must VCC input



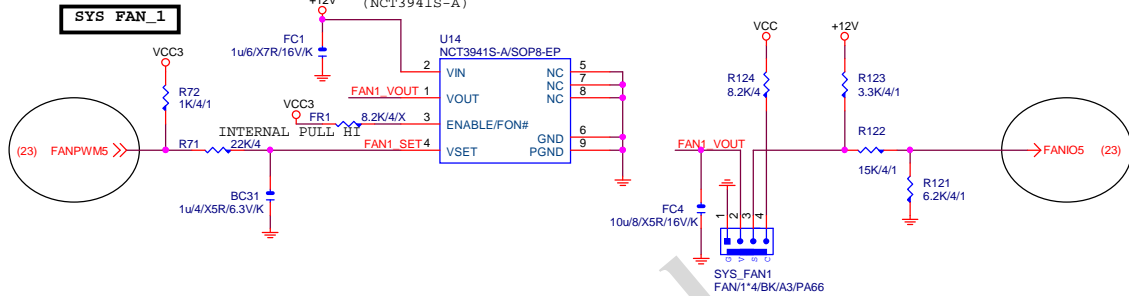
The division voltage of VIN2 & VIN3 must be around 2.9V

# CPU SMART FAN

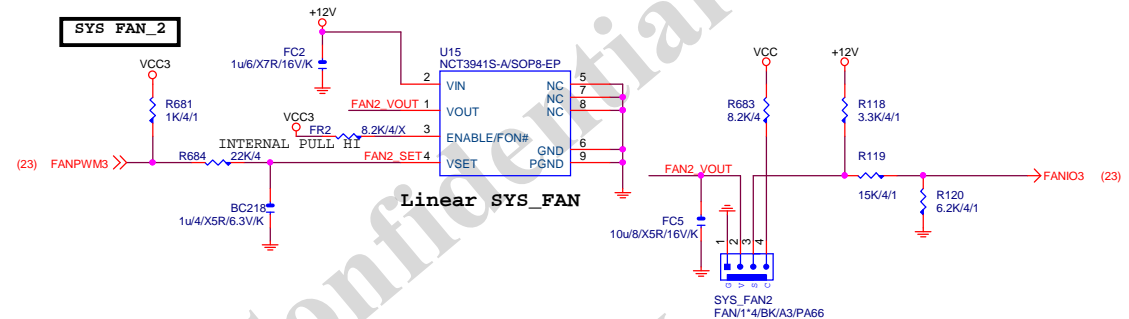


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## Linear SYS\_FAN

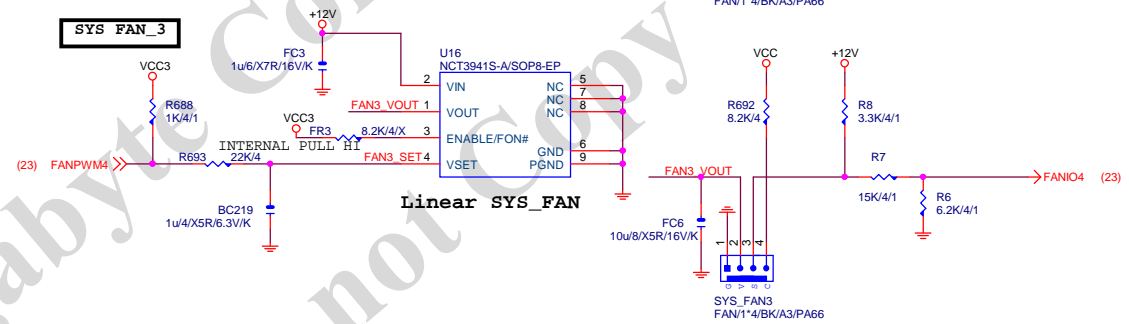


## SYS\_FAN\_2



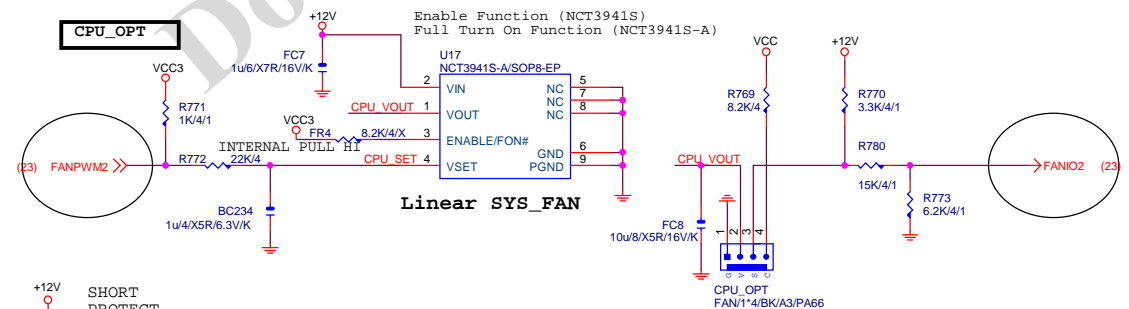
## Linear SYS\_FAN

## SYS\_FAN\_3

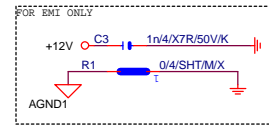
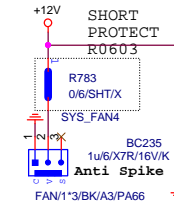


## Linear SYS\_FAN

## CPU\_OPT



## Linear SYS\_FAN

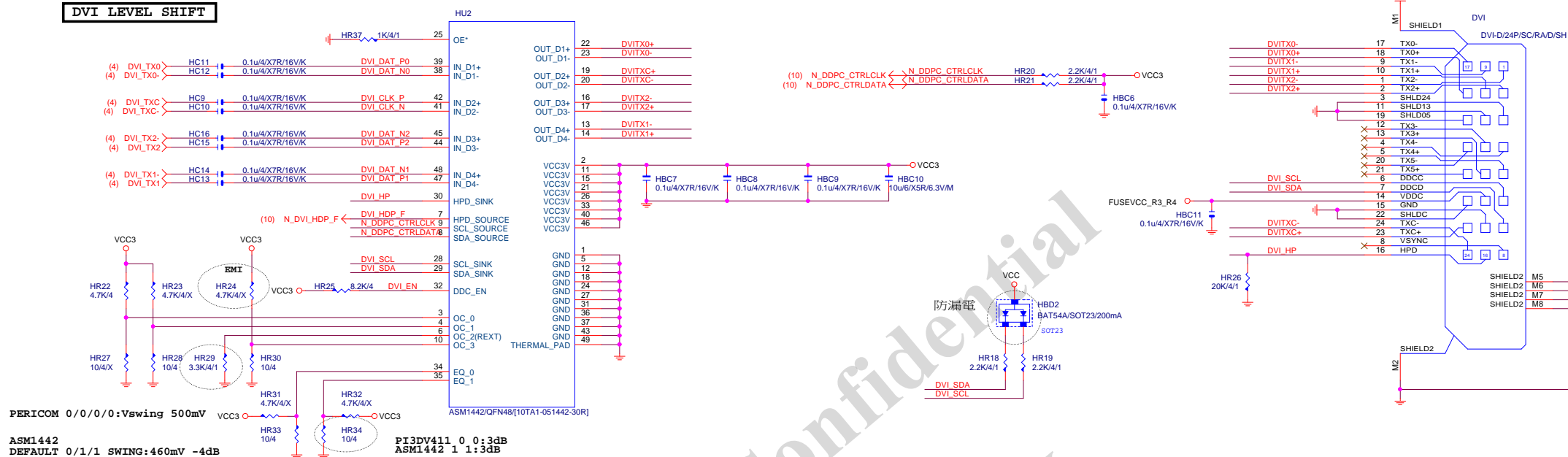


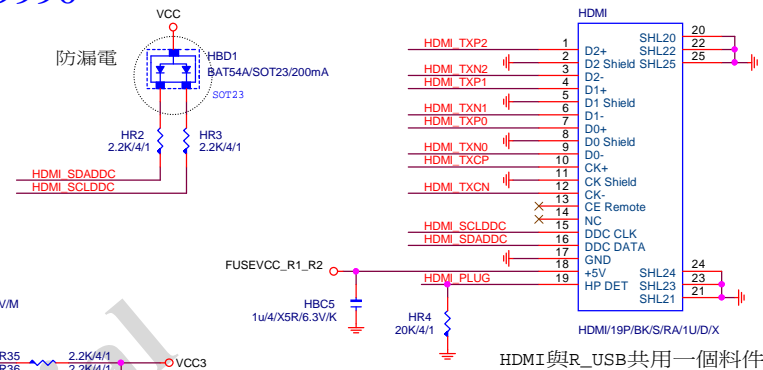
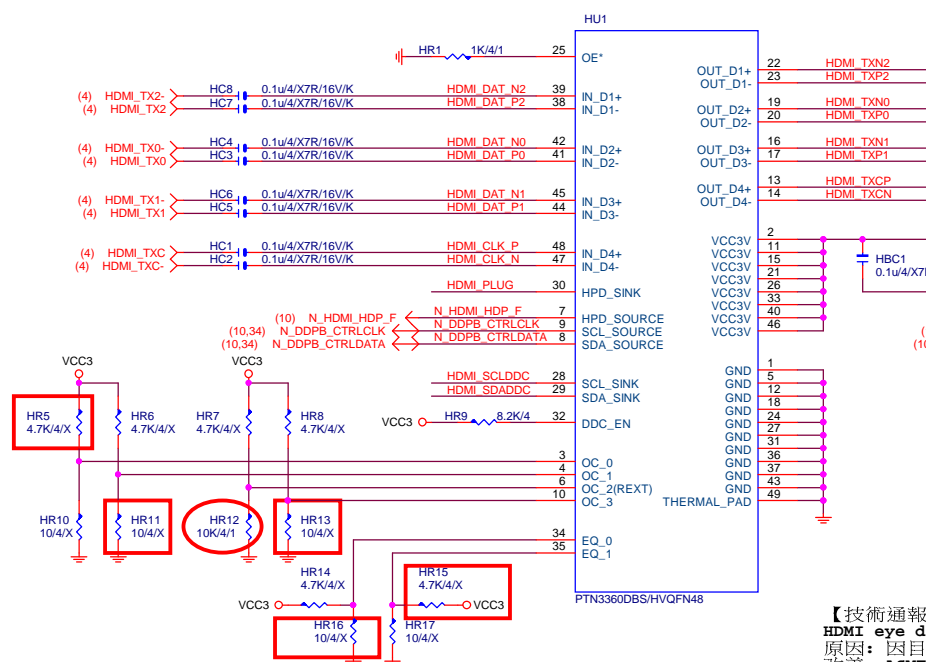
## Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.11	
Date:	Wednesday, July 16, 2014	Sheet	32 of 45



## DVI LEVEL SHIFT





HDMI與R\_USB共用一個料件

【技術通報R&amp;D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

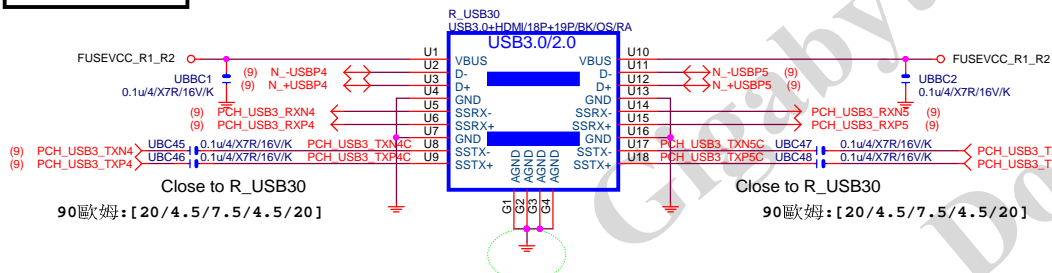
原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K

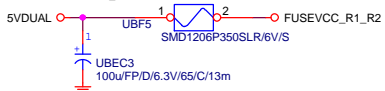
ASM1442:紅色框要上,HR12:3.16K

## USB30\_20 CONNECT



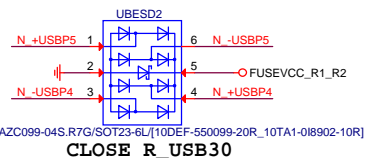
USB30	PWR
-------	-----

Polyswitch-1206

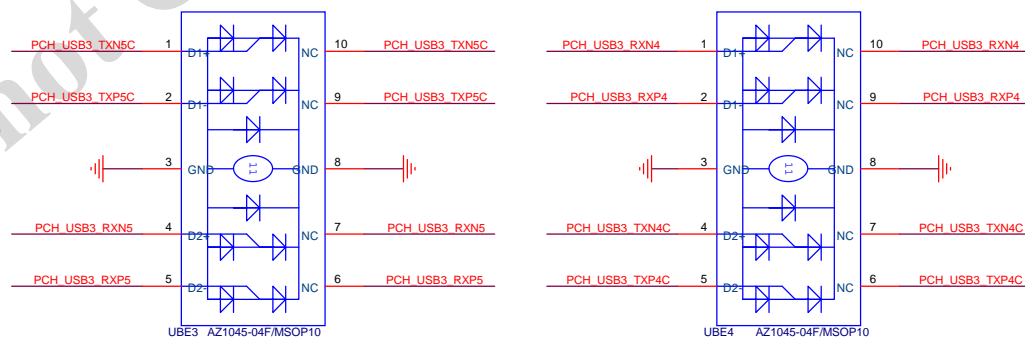


USB3.0 1Port - 1Fuse (3.5A)

## USB20 ESD PROTECT

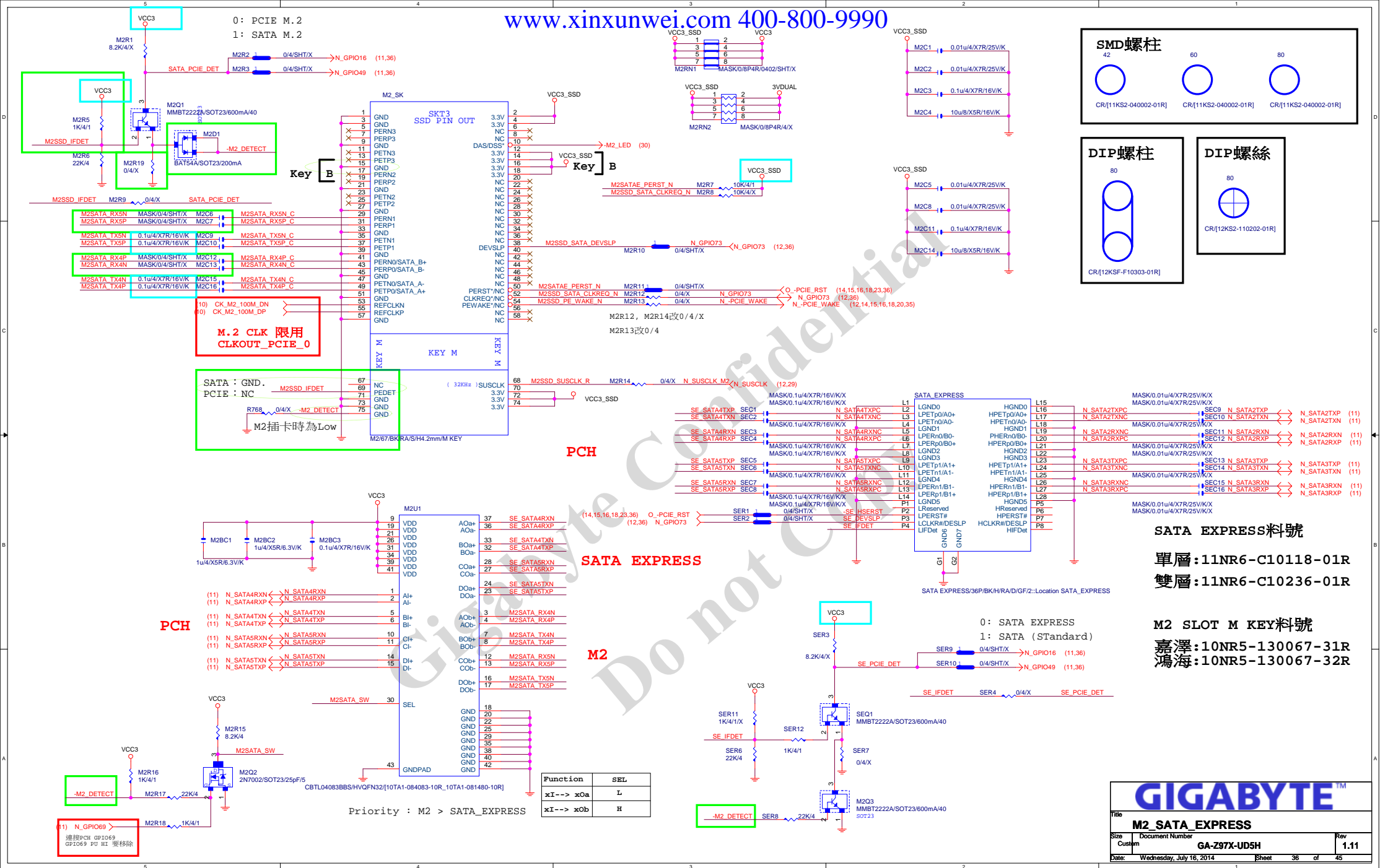


USB30 ESD PROTECT

**GIGABYTE™**

Title			
<b>HDMI</b>			
Size	Document Number	Rev	
Custom	<b>GA-Z97X-UD5H</b>	<b>1.11</b>	
Date:	Wednesday, July 16, 2014	Sheet	34 of 45

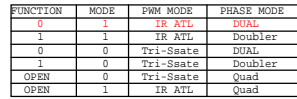




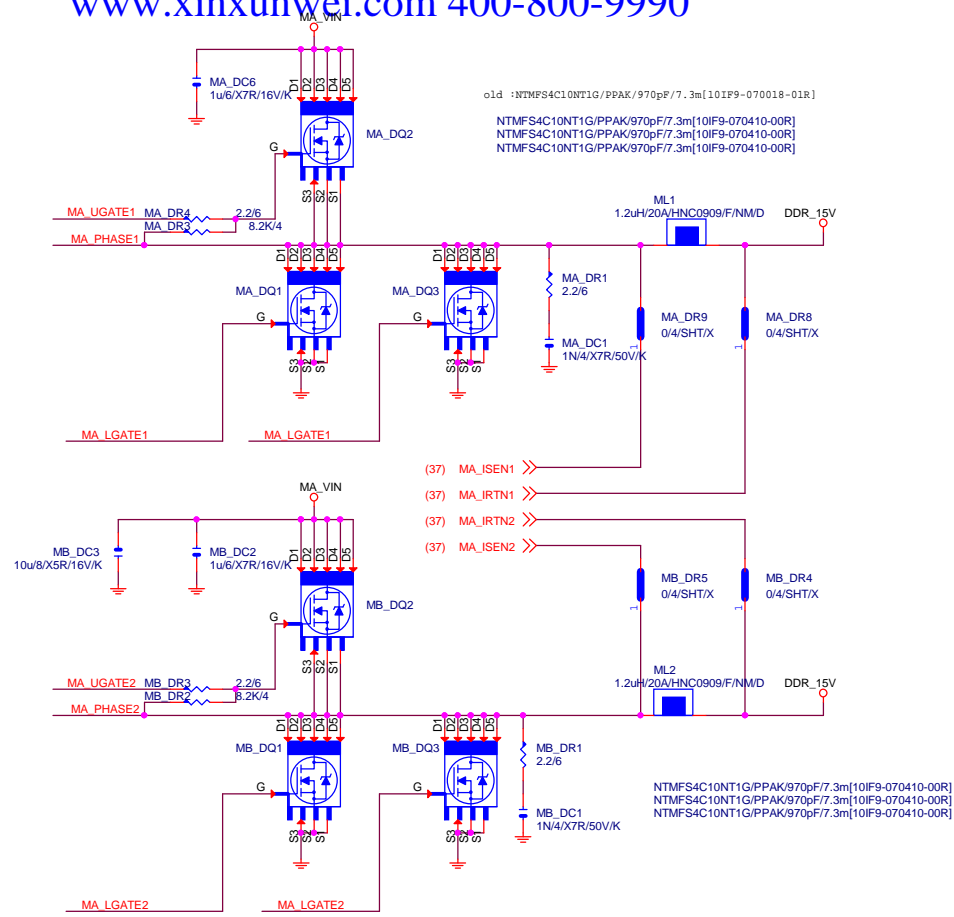
**GIGABYTE™**

Title			
<b>M2_SATA_EXPRESS</b>			
Size	Document Number	Rev	
Custom	<b>GA-Z97X-UD5H</b>	<b>1.11</b>	
Date:	Wednesday, July 16, 2014	Sheet	36 of 45

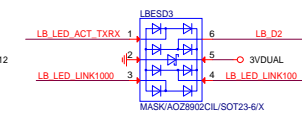
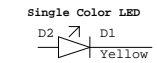


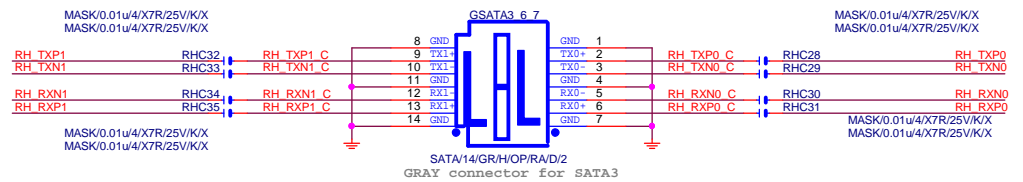
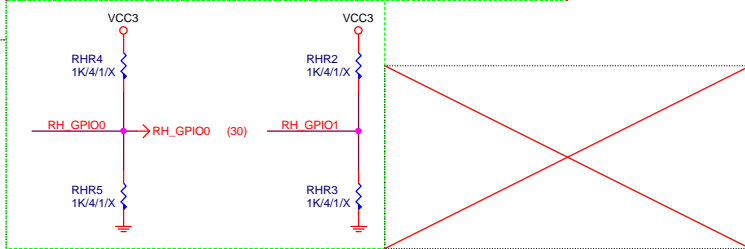
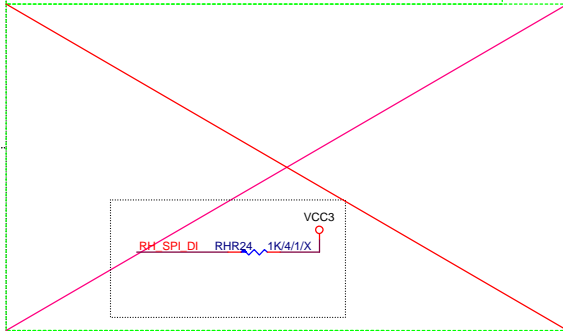
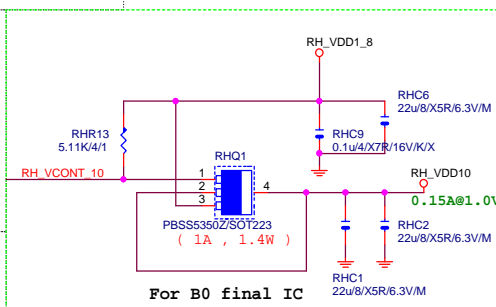
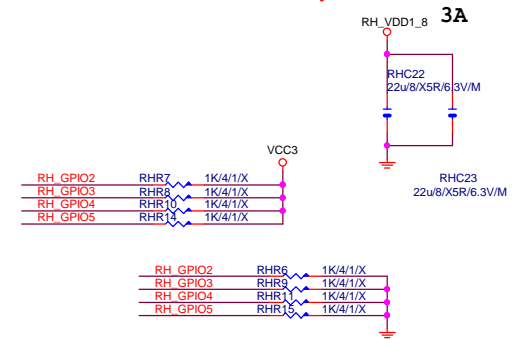
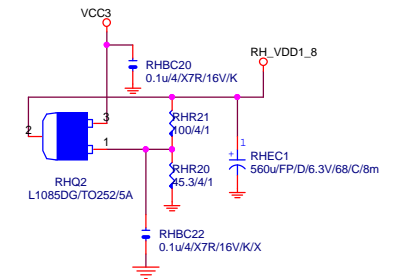
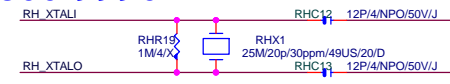
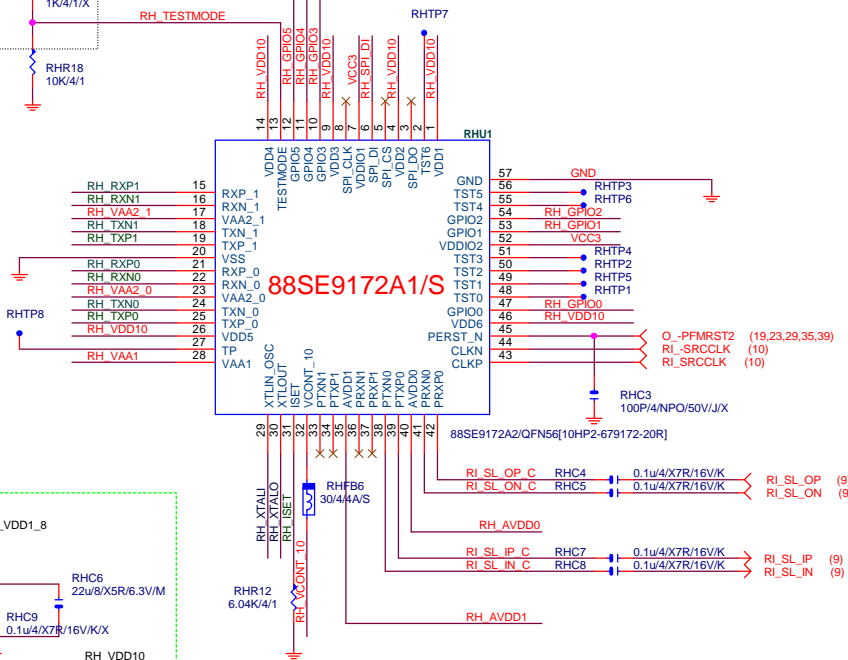
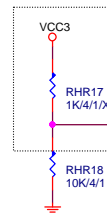
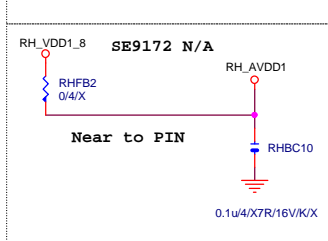
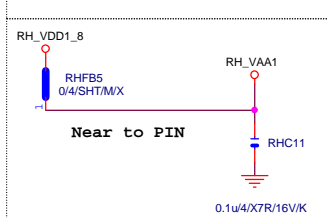
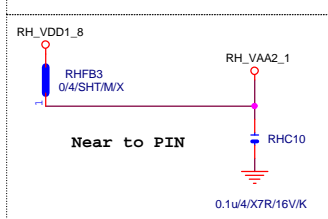
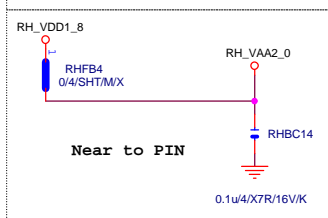
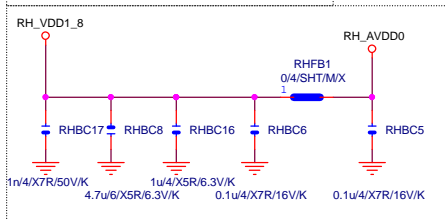
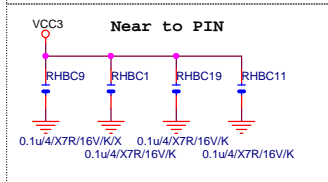
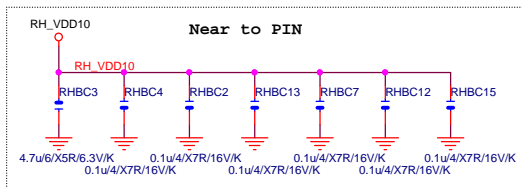


The schematic diagram illustrates the power supply for the MA3000 module. It features a 5VDUAL input connected to a network of capacitors (MAC13, MAC17, MAC21, MAC22, MAEC3, MAEC4, MAEC1, MAEC2) and inductors (ML3, MA). A 'Close Choke' block is shown, and a 'Close MOS' block is indicated. The output is MA\_VIN, which is connected to the MA\_D1 pin of the MA3000 module. A 12V input is also shown connected to the MA\_D1 pin.







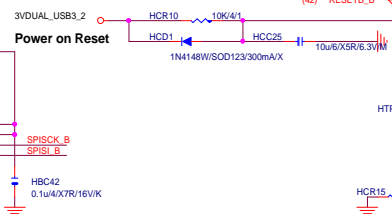
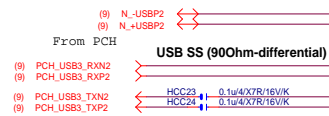
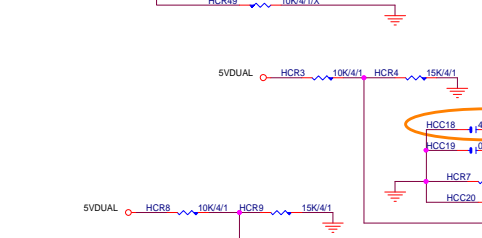
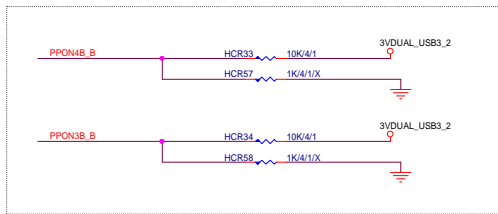


90歐姆:[15/4.5/7.5/4.5/15]

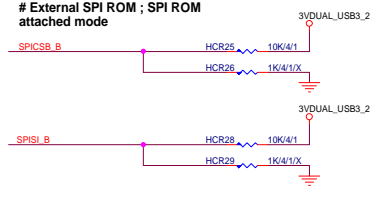
Marvell 9172 Power Requirements  
Analog 1.8V 230mA  
Core 1.0V 900mA  
I/O 3.3V 50mA

## # Number of Ports ; 4Ports mode

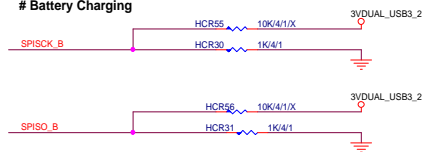
PPON3B / PPON4B : H / H ( 4 port )  
PPON3B / PPON4B : L / L ( 2 port )



## # External SPI ROM ; SPI ROM attached mode



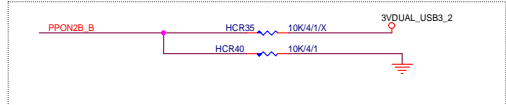
## # Battery Charging



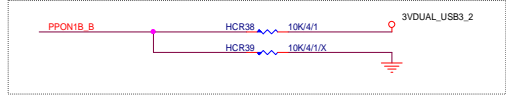
Put close to U1  
Do check with crystal vendor  
if the value of C31, C32 and R31 are all appropriate.

Put close to U1  
Short and broad connection to GND  
Don't split R32 into multiple resistors.

## #5 VBUS Power Control ; Individual mode



## # PPON1B Pin Function ; Port1 PPONB mode

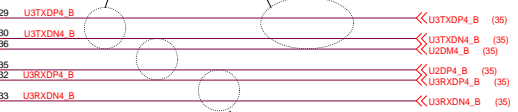


uPD720210

## USB HS (90Ohm-differential)

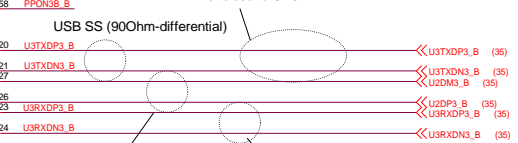
## USB SS (90Ohm-differential)

Put close to CN4



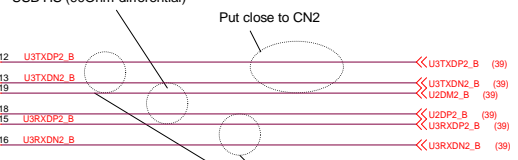
## USB SS (90Ohm-differential)

Put close to CN3



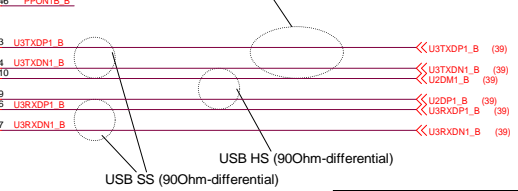
## USB SS (90Ohm-differential)

Put close to CN2

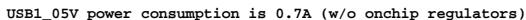


## USB SS (90Ohm-differential)

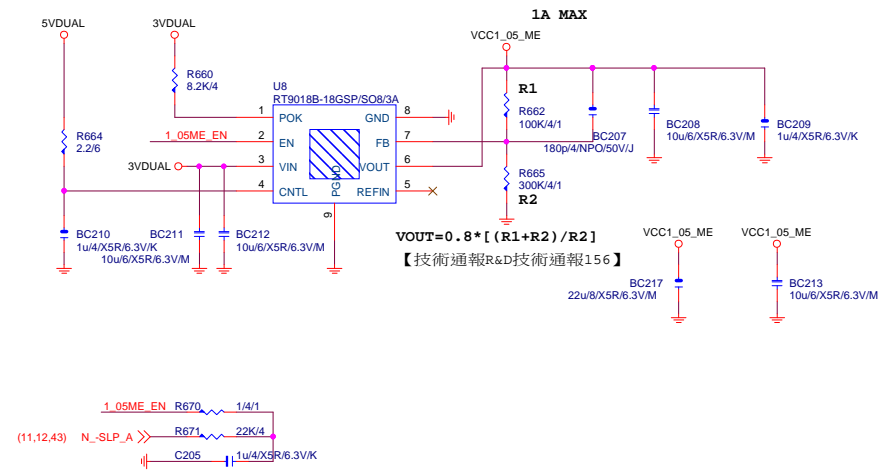
Put close to CN1



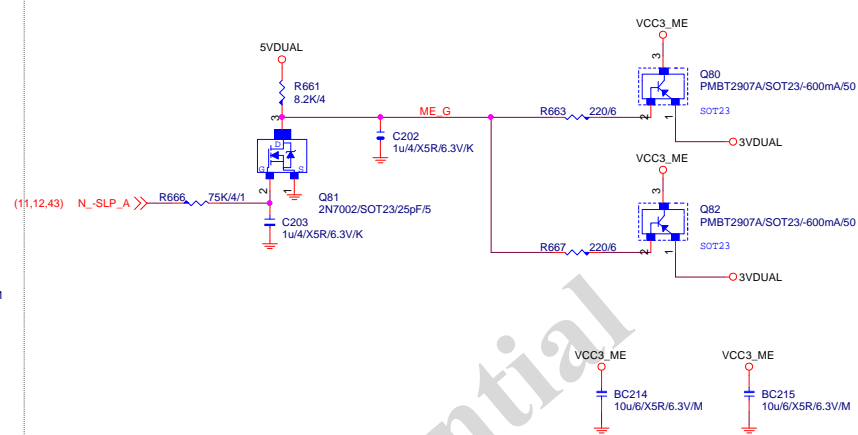
GIGABYTE™			
Title			
D720210 4port Hub_B			
Size	Document Number	Rev	
C	GA-Z97X-UD5H	1.11	
Date	Wednesday, July 16, 2014	Sheet	41 of 45



VCC1\_05\_ME



VCC3\_ME1

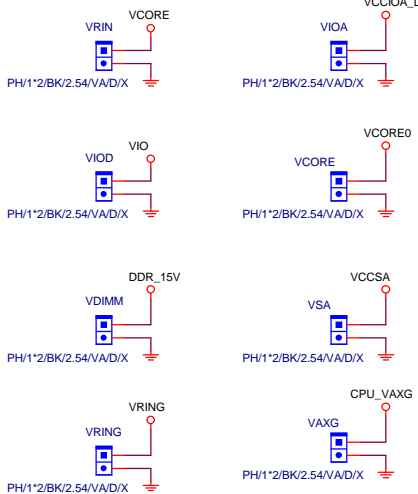
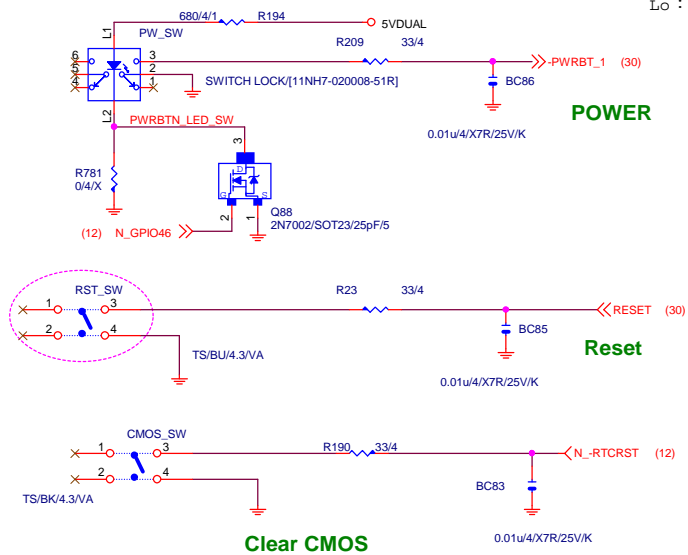


Gigabyte Confidential

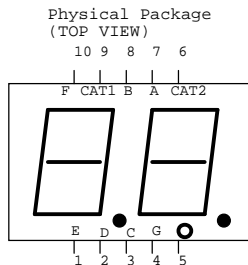
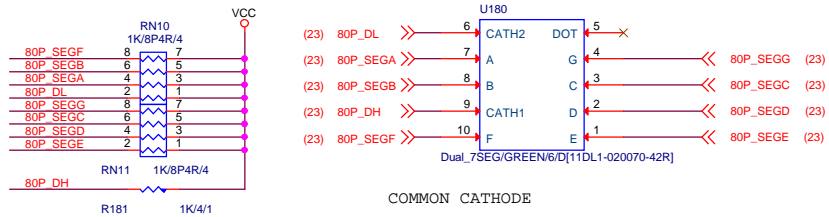
Do not Copy

**GIGABYTE™**

Title			DDR15V / M3 POWER
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.11	
Date:	Wednesday, July 16, 2014	Sheet	43 of 45



## 80 PORT



# GIGABYTE™

Title <b>RST, PWR, CLR_CMOS, OV</b>		
Size Custom	Document Number <b>GA-Z97X-UD5H</b>	Rev <b>1.11</b>
Date: Wednesday, July 16, 2014	Sheet 44	of 45



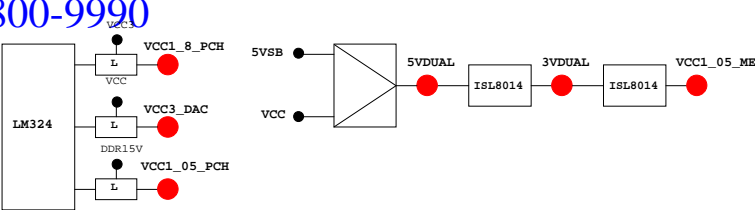
PCB GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPIO0	N/A
GP1/TACH1	MAIN	GPI	GPIO1	N/A
GP2/PIRQE#	MAIN	GPI	~PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	GPI	~PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	GPI	~PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	GPI	~PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN	MAIN	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPIO8	N/A
GP9/OC5#	STBY	NATIVE	USB OC5#	N/A
GP10/OC6#	STBY	NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY	NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12
GP13	STBY	L	GPI	LPCPME#
GP14/OC7#	STBY	NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)
GP16	MAIN	MAIN	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN	MAIN	GPIO17	P/U 8.2K VCC3
GP18	MAIN	MAIN	GPIO18	P/U 8.2K VCC3
GP19	MAIN	MAIN	GPIO19	P/U 8.2K VCC3
GP20	MAIN	MAIN	GPIO20	P/U 8.2K VCC3
GP21	MAIN	MAIN	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPIO22	P/U 8.2K VCC3
GP23	MAIN	MAIN	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#
GP25	STBY		Mobile Only	N/A
GP26	STBY		Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27
GP28	STBY	H	GPO	PWR LED
GP29	STBY	L	GPI	GPIO29
GP30	STBY	H-Z	GPI	Mobile Only
GP31	STBY	H-Z	GPI	Mobile Only
GP32	MAIN	H	GPO	N/A
GP33	MAIN	H	GPO	N/A
GP34	MAIN	H-Z	GPI	~PCI_STOP
GP35	MAIN	L	GPO	~ACZ_DET
GP36	MAIN	GPI	N/A	N/A
GP37	MAIN	GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect
GP39	MAIN	H-Z	GPI	GPIO39
GP40	STBY	NATIVE	USB OC1#	N/A
GP41	STBY	NATIVE	USB OC2#	N/A
GP42	STBY	NATIVE	USB OC3#	N/A
GP43	STBY	NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44
GP45	STBY	NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46
GP47	STBY		Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48
GP49	MAIN	H-Z	IN	GPIO49
GP50	MAIN	NATIVE	~REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	~GNT1
GP52	MAIN	NATIVE	~REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	~GNT2
GP54	MAIN	NATIVE	~REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	~GNT3
GP56	STBY	NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1
GP58	STBY	H-Z	NATIVE	F_USB_OC
GP59	STBY	NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)
GP61	STBY	L	NATIVE	~SUSTAT
GP62	STBY	L	NATIVE	SUSCLK
GP63	STBY	L	NATIVE	GPIO63
GP64	MAIN	L	NATIVE	CLKOUTFLEX0
GP65	MAIN	L	NATIVE	CLKOUTFLEX1
GP66	MAIN	L	NATIVE	CLKOUTFLEX2
GP67	MAIN	L	NATIVE	CLKOUTFLEX3
GP72	STBY	H-Z	NATIVE	VCORE_OV4
GP73	STBY		Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2
GP75	STBY	H-Z	NATIVE	N/A(Reverse)

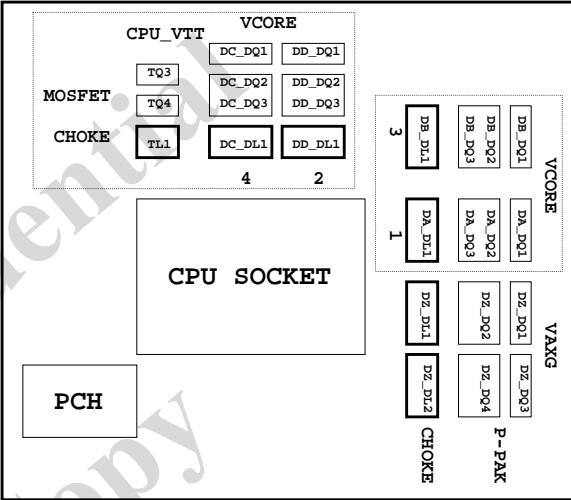
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	SE_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRT2X/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

散熱模組料號：

Z77--D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

Gigabyte Technology			
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